
**VARIABLE FREQUENCY
THREE PHASE THYRISTOR FIRING BOARD
Model FCOVF6100****INTRODUCTION**

The FCOVF6100 board was developed at the request of locomotive equipment manufacturers. Presently, the principal applications of the board are in off-road vehicle battery chargers and generator exciters for locomotives and utility power generators.

The FCOVF6100 responds to a voltage or milliamp current signal to produce a delayed set of 60° spaced high current thyristor gate pulses.

The variable frequency firing board is a modification of the industry standard 50/60 Hz FCOG6100 firing board, of which approximately 55,000 are in service in various industrial applications. The modifications involve the use of a dc/dc converter to derive SCR gate and logic power and added circuitry to make the gate delay angle insensitive to ac supply frequency.

APPLICATIONS

A programming plug adapts the board to suit various types of thyristor controllers or converters (rectifiers).

The range of applications is enhanced by the use of Auxiliary Firing Board's and regulators.

PERFORMANCE SPECIFICATIONS

Key firing board specifications are:

- Gate drive: Picket-fence with an initial 'hard firing' pulse of: 15.0 V open circuit, 1.8 A short circuit and a sustaining pulse of: 7.0 V open circuit, 0.5 A short circuit. The frequency of the picket-fence is 384 times the mains frequency.

- Phase balance $\pm 1.0^\circ$
- Gate isolation +3500 V-pk
- Gate inhibit: soft-start/soft-stop and instant-start/instant-stop
- Phase loss inhibit
- High immunity to mains voltage distortion
- Phase sequence insensitive
- Fused gate pulse modules
- Enable status output

The gate delay angle varies in negative proportion to the delay angle command voltage.

TECHNICAL INFORMATION**Board Power**

Standard firing board power obtained via a DC-DC converter. This converter is rated for a 15 watt ± 15 Vdc output with a 20 to 60 Vdc input. The rated input/output voltage isolation is 500Vdc. The converter input voltage is limited to 45 Vdc by a zener diode pre-regulator. The -15 Vdc output is connected to circuit common in order to provide +15 Vdc and +30 Vdc outputs with respect to circuit common.

Optionally the DC-DC converter can be omitted and regulated +30 Vdc can be supplied from an external source.

Gate Delay Phase References

Note: This explanation assumes a 30 Hz to 120 Hz operating range.

The phase references for the phase locked loop (PLL) delay angle generator are derived from the three phase line which is present on the firing board at the gate trigger transformers. These voltages are processed by resistive attenuators, low pass filters, phasor

addition circuitry, and differential comparators.

The time constant of the low pass filter is selected to give a lagging phase shift of 60° at the 60 Hz operating frequency. A phasor addition circuit adds a 60° phase lead, giving an adjusted reference delay phase shift at 60 Hz of $60^\circ - 60^\circ = 0^\circ$. Because of the frequency dependence of the phase reference low pass filter, the adjusted phase angle ranges from a phase lead of $41^\circ - 60^\circ = -19^\circ$ at 30 Hz to a phase lag of $74^\circ - 60^\circ = 14^\circ$ at 120 Hz.

Gate Delay Angle Generator

The three square wave 50% duty cycle phase reference signals from the phase reference circuitry are applied to EX-OR phase comparators in the LSI device along with three delayed phase references from the output of the PLL delay angle generator. External to the LSI device, a gate delay angle command voltage is summed with the outputs of the three phase detectors and low pass filtered by an inverting amplifier. This inverted voltage sum is applied to the control input of the LSI device where it is designated as the Voltage Controlled Oscillator (VCO) control voltage.

At a given reference frequency, the sum of the control signal and the phase detector outputs is constant, as required to maintain the VCO in phase lock with the line frequency. Thus an increase in the control voltage must be accompanied by a like decrease in the sum of the phase detector outputs. The delay angle between the three phase references and the three delayed output phase references of the PLL, which are input pairs to the three EX-OR phase detectors, is thus forced to track the control voltage.

Frequency Insensitivity

The firing circuit gate delay angle is made insensitive to the line frequency by a modification of the PLL VCO, as described below.

The VCO frequency is proportional to the current in the VCO timing resistor R. For the usual fixed frequency operation, the sink for the current in R is the circuit common. The

result is that the resistor current and the VCO frequency are proportional to the voltage across R.

The variable frequency modification consists of terminating R in a voltage source instead of the usual circuit common.

The output of this voltage source varies in negative proportion to the line frequency. In this way, the voltage across the frequency determining resistor increases with the line frequency with no increase in the sum of the phase detector outputs and the control voltage. Thus the PLL delay angle changes by only about 3° over a frequency range of 30 Hz to 120 Hz.

Net Gate Delay Angles

The net gate delay angle is the sum of the adjusted reference signal phase shift ϕ and the PLL delay angle α_p as:

$$\alpha_{net} = \alpha_p + \phi$$

The PLL delay angle range over the operating frequency range is shown in the table below.

F(Hz)	30	60	120
α_{p-min} (deg)	11	12	13
α_{p-max} (deg)	154	155	158
$\phi - 60$ (deg)	-19	0	14
α_{n-min} (deg)	-8	12	27
α_{n-max} (deg)	135	155	172

Gate Pulse Amplifier

The PLL and associated decoding logic produce six sets of equidistant SCR gate pulses. The user can select a 120° gate pulse burst or two 30° wide bursts spaced by 30° .

Circuitry consisting of a transistor array, resistors, capacitors, and gate pulse isolation transformers amplify and shape the SCR gate current pulses. Each pulse module consists of a 2:1 ratio pulse transformer tested at 3500 Vrms isolation, two secondary diodes, noise suppression resistors across the primary and

across the gate drive output, and a fuse in series with the output.

Typical peak SCR gate current is 1.0 A with a rise time of 0.5 A in 0.5 μ s.

Soft-start/Soft-stop times

The following information is provided to assist the customer in determining the operating characteristics of the firing board. It is recommended that an Enerpro applications engineer be consulted prior to adjusting component values. Component designations apply to schematic E0445 Rev. G.

Soft-start time is calculated as follows:

$$t = (1.5 + R21 + R22)(C9)(0.579)$$

$$t = s, R = M\Omega, C = \mu F$$

NOTE: Normally installed values of 100 k Ω , 10.0 k Ω and 22 μ F will yield a soft -start time of: $t = 1.40$ s.

The soft-stop time is dependent upon the value of R22 and C9. This value can also be adjusted as necessary and can be calculated as follows:

$$t = (R22)(C8)(1.84)$$

$$t = ms, R = k\Omega, C = \mu F$$

NOTE: Normally installed values will yield a soft -stop time of: $t = 0.40$ s.

Circuit Board

The FCOVF6100 is assembled at the Enerpro plant in Goleta, California. The circuit boards are made by a UL listed fabricator from 0.093 in. (2.36 mm) thick FR4 fire-resistant epoxy-

glass laminate. Creepage distances conform to UL 508 and VDE 0110. Boards are conformal coated (MIL-1-46058 [Type UR]), and are designed for operation from 0°C to +75°C.

Board dimensions are 6.0 in. (152 mm) by 7.5 in. (190 mm). Corner mounting holes are spaced 5.625 in. (143 mm) by 7.125 in. (181 mm).

Rugged AMP Mate-N-Lok™ connectors are used for customer interfaces. These connectors simplify maintenance and troubleshooting. Additional MTA style connectors are provided to facilitate interfacing between Enerpro boards.

Additional Information

Please contact an Enerpro applications engineer to discuss your requirements or to request additional information.

The following is a partial listing of complimentary data sheets:

- Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.
- R157 Auxiliary Firing boards.
- CVR600 brochure - constant voltage / constant current regulator package.

Ordering Information

Please contact Enerpro, 7 a.m. to 5 p.m. Monday through Friday, for assistance or use the attached "how to order" worksheet to determine the correct part number.

HOW TO ORDER

Select the circuit board configuration that suits your application from the table below:

Model Number	Variable Frequency Three Phase Firing Board					
	Code	Thyristor Circuit Arrangement				
	01	AC Controllers:				
	02	DC Converter				
		Code	Paralleled Thyristors			
		0	= No			
		1	= Yes			
		Code	Frequency Range			
		01	30 Hz to 120 Hz.			
		02	Other - Please specify.			
		Code	Maximum Thyristor Input Voltage			
		XX	= Voltage ÷ 10 (e.g., 48 = 480 V, etc.)			
		Code	Power Connection			
		0	Without DC-DC Converter			
		1	With DC-DC Converter			

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Please contact an Enerpro applications engineer if you have any questions.

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