

## OPERATING MANUAL FOR SIX-SCR GENERAL PURPOSE GATE FIRING BOARD, PART NO. FCOG6100 REVISION R

### INTRODUCTION

This manual is intended to familiarize the user with the salient features and specifications of the firing board. A simple checkout procedure is included together with typical firing circuit signal waveforms.

### PRODUCT DESCRIPTION

#### 1.0 Application

The general purpose firing board responds to a voltage or milliamp current signal to produce a delayed set of six 60° spaced high current SCR gate pulses. Different configurations are available upon ordering to suit various types of SCR controllers or converters (rectifiers or inverters).

#### 2.0 LSI Logic Device

All firing circuit logic is contained in a custom 24-pin CMOS LSI gate array. Additional detail on the firing circuit theory is contained in an engineering society paper<sup>1</sup>.

#### 3.0 Board Mounted Connectors

The firing board is completely connectorized to simplify maintenance and troubleshooting.

##### 3.1. Gate/Cathode Connectors

The SCR gate/cathode interface is provided by 8-position Mate-N-Lok™ right-angle headers<sup>2</sup>, J1 and J2, and mating plugs, P1 and P2. The jacks are keyed to prevent incorrect installation of the mating plugs. Plug P1 accesses the gates and cathodes of the three SCRs having load connected cathodes when the SCRs are arranged in the in-line ac controller or bridge converter configurations. Similarly, plug P2 accesses the gates and cathodes of the three SCRs having line-connected cathodes. Plug P1 or P2 and the associated cable are omitted when the firing board is used with 3-SCR/3-diode circuits.

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<sup>1</sup> Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.

<sup>2</sup> Vertical headers are available upon request.

### **3.2. Control Signal Connector**

The firing board connects to the gate delay command and inhibit controls through a 12-position Mate-N-Lok™ connector designated as J3. This connector also accesses the outputs of the 24 Vac board mounted transformer (if specified), the 30 VDC rectifier, and the regulated +12/+5 VDC outputs.

### **3.3. Optional Power Supply Excitation**

The board-mounted 24 VA power supply transformer is normally energized by on-board connection to two of the mains voltages which appear at positions 5 and 8 of header J2. When the SCRs are powered from non-standard voltages, the board mounted power supply transformer can be energized through the optional 5-position Mate-N-Lok™ plug/header, P4/J4.

The 24 Vac and 30 VDC connections on the control signal connector, J3, permit the board to be powered from an external source if no onboard transformer is specified. With the board-mounted transformer installed, approximately 10 watts of ac or DC power is available from J3 to power lamps or control relays.

### **3.4. Optional Reference Connector**

In certain applications, the ac mains voltage may not be present at the SCR cathodes or the ac voltage may go to zero during load faults<sup>3</sup>. In these cases, or when galvanic isolation is required between power and control circuits, external phase reference voltages are applied through optional Mate-N-Lok™ plug P5. The mating header, J5, and voltage sensing resistors R6, R7 and R8 are installed on the board space normally occupied by power supply transformer T1. Board power is then obtained externally from 24 Vac or 30 VDC applied through P3/J3.

### **3.5. Test Signal Input Connector**

A 3-position cable header, J7, is used to inject low level 3-phase test reference signals from a firing board test fixture into the delay determinator circuit. This allows the board checkout to proceed without connection to high voltage power. In addition, a three-position Mate-N-Lok™ connector, P7, is available for this purpose or for connection of externally attenuated phase reference signals. The use of P7 and external attenuating resistors allows the use of the onboard transformer while still providing connection to external phase references.

### **3.6. Auxiliary Regulator Board Connector**

Key firing board signals are brought out to a 20-position ribbon cable connector socket, J6, for interfacing with a second printed circuit board which can be conveniently mounted on stand-offs above the firing board. This regulator board can provide various closed-loop functions (torque,

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<sup>3</sup> For example, in a 6-SCR interphase transformer converter or an arc welder converter.

speed, position voltage, power, etc.) and diagnostic circuitry. The 20-position connector socket also facilitates board testing.

### 3.7. GATE DELAY COMMAND

The gate delay command signal, SIG HI, may be configured either as a 4 to 20 mA current command or one of several voltage commands, the default being 0 to 5 Volts. The input resistance presented to the delay command signal SIG HI is determined by resistor R30. This value is selected as 10.0 k $\Omega$  when the control signal is designated as a control voltage. The buffer amplifier resistance table below delineates the required resistor values to accommodate different command signal levels. Alternatively, refer to the schematic diagram, E128, revision R.

Table 1. SIG HI Range vs. Buffer Amplifier Component Values

SIG HI Range	Resistance (in k $\Omega$ unless noted)					
	R16	R19	R25	R26	R27	R30
0 to 5 V	100	32.4	130	46.4	1.00M	10.0
0.85 to 5.85 V	100	32.4	196	46.4	1.00M	10.0
0 to 10 V	100	32.4	1.00M	90.9	750	10.0
0 to 2 V	274	32.4	78.7	47.5	1.00M	10.0
4 to 20 mA	100	32.4	130	47.5	1.00M	249 $\Omega$

### 4.0 GATE INHIBITS

SCR gating is inhibited by making either or both of the inhibit signal points, designated as  $\overline{I_1}$  and  $\overline{I_2}$  appearing at J3 (pins 4 and 12 respectively) a logic zero.

In the case of the instantaneous inhibit,  $\overline{I_1}$ , resistor R32 (1.50 k $\Omega$ ) on the firing board is provided to pull the  $\overline{I_1}$  signal point low if the connection between  $\overline{I_1}$  and +12 VDC is opened. This ensures that SCR gating is inhibited if plug P3 is inadvertently disconnected. In applications where the instantaneous gate inhibit function is not utilized, a jumper wire is installed between pins 4 and 6 of P3 to hold  $\overline{I_1}$  at +12 VDC when P3 is installed in J3.

The inhibit signal  $\overline{I_2}$  is connected to +12 VDC through pull-up resistor R31 (1.50 k $\Omega$ ) on the firing board. When  $\overline{I_2}$  is grounded, the gate delay angle is ramped to the maximum delay angle before gating is inhibited. This is termed the soft-stop shutdown mode. Removing the ground on  $\overline{I_2}$  causes gating to be enabled with the delay angle set to the maximum limit. The delay angle then ramps down to the commanded angle. This is termed the soft-start turn-on mode. The soft-stop and soft-start periods are

determined by two timing resistors and a capacitor.

## 5.0 PHASE-LOSS INHIBIT

A phase loss circuit operates to instantly inhibit SCR gating if the mains phase balance is abnormal or, in the extreme case, if one phase voltage is missing. Gating is enabled when the proper phase balance is restored: gating initiates at the maximum delay angle, and ramps down to the commanded angle at a rate determined by the soft-start RC time constant. The FCOG6100 revision R product features a new, enhanced phase loss detection circuit that is immune to line frequency variations and transient voltages on the SIG HI line.

The phase-loss inhibit circuit is also activated when three phase power is initially applied to the SCRs. Gating is inhibited until the power supply voltage has stabilized. Gating then commences at the delay angle limit and ramps down to the commanded angle at a rate determined by the soft-start RC time constant.

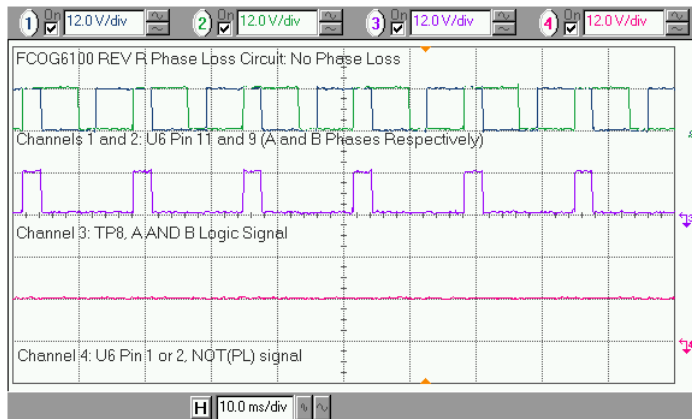


Figure 1. Phase Loss Circuit Signals – No Phase Loss<sup>4</sup>

- Channels:
1. Digital A Phase Reference Signal, U6 P11
  2. Digital B Phase Reference Signal, U6 P9
  3. A and B logic signal, TP8
  4.  $\overline{\text{PL}}$  Signal, U6 P1

<sup>4</sup> All waveforms contained in this document were obtained with the FCOG6100 revision R firing board connected to 240 Vac, 60 Hz, balanced 3-phase power via sockets 2, 5, and 8 of plug P2. The time base of each screenshot has been calibrated for phase measurements as noted at 60 Hz. All component designations refer to drawing E128, revision R.

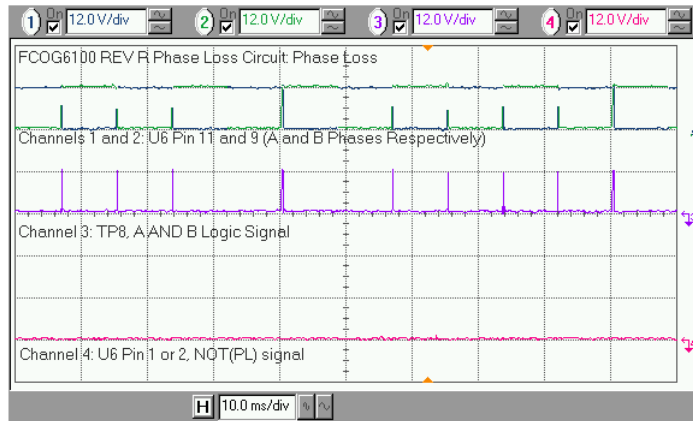


Figure 2. Phase Loss Circuit Signals – Phase Loss  
 Channels: 1. Digital A Phase Reference Signal, U6 P11  
 2. Digital B Phase Reference Signal, U6 P9  
 3. A and B logic signal, TP8  
 4.  $\overline{PL}$  Signal, U6 P1

## 6.0 REFERENCE PHASE ANGLE SELECTION

Phase shifting the mains phase references by  $0^\circ$  (for controller applications) or by  $30^\circ$  lagging (for converter applications) is achieved by a first-order RC low-pass filter formed by RN6 and C15, C16, and C18. For  $30^\circ$  lagging references, the previously referenced capacitors are  $0.033 \mu\text{F}$  film capacitors and RN6 is a  $120 \text{ k}\Omega$ , three-position, isolated SIP resistor network.

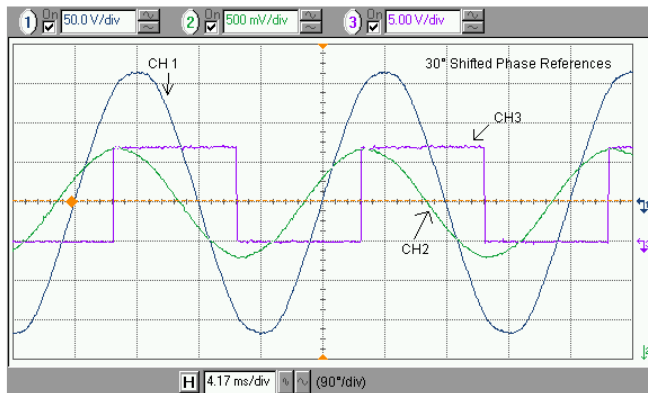


Figure 3. Thirty-degree shifted phase references, Phase A  
 Channel: 1. Phase A Line-to-Neutral Voltage  
 2. Attenuated and Filtered Mains Voltage at RN6-3  
 3. Reference Comparator Output, TP5

For  $0^\circ$  references,  $0.01 \mu\text{F}$  film capacitors may be installed with  $\text{RN6} = 120 \text{ k}\Omega$ . Alternatively,  $0.033 \mu\text{F}$  film capacitors may be used with a  $33 \text{ k}\Omega$ , three-position, isolated SIP resistor network installed for RN6. The latter is a preferred scheme if the FCOG6100 may be used as a controller or a converter. This is due to the fact that the three capacitors forming the phase shift network must be matched to within  $\pm 1\%$  to ensure uniform shift on each phase. Changing RN6 to change phase shift is a more reliable scheme than changing three precision-matched capacitors; RN6 may be provided in a socket for user convenience if controller or converter operation is desired with one unit.

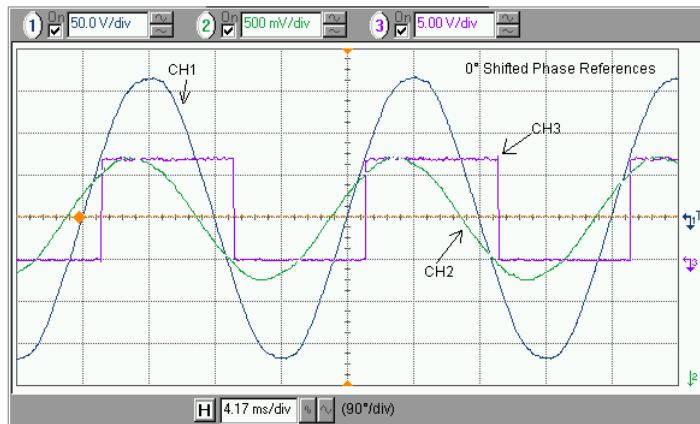
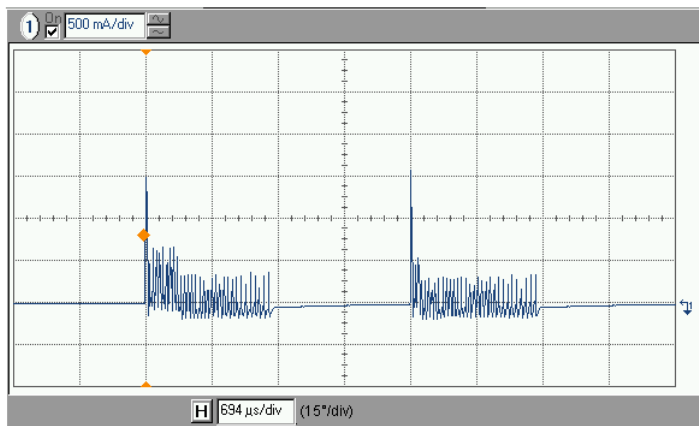


Figure 4. Zero-degree shifted phase references, Phase A  
 Channel:      1. Phase A Line-to-Neutral Voltage  
                   2. Attenuated and Filtered Mains Voltage at RN6-3  
                   3. Reference Comparator Output, TP5

## 7.0 GATE PULSE PROFILE SELECTION

A two-position jumper, JU1, enables selection of gate pulse profile. With JU1 installed, the pulse profile is two  $30^\circ$ -wide bursts, each with an initial hard-firing gate pulse, followed by sustaining “picket fence” pulses. With the jumper omitted, the gate pulse profile changes to a single  $120^\circ$ -wide burst with the same hard-firing initial pulse. The initial hard-firing pulse and sustaining pulses help ensure proper SCR conduction.



Figure<sup>5</sup> 5. 2-30° Gate Pulse Profile (Into 1Ω).

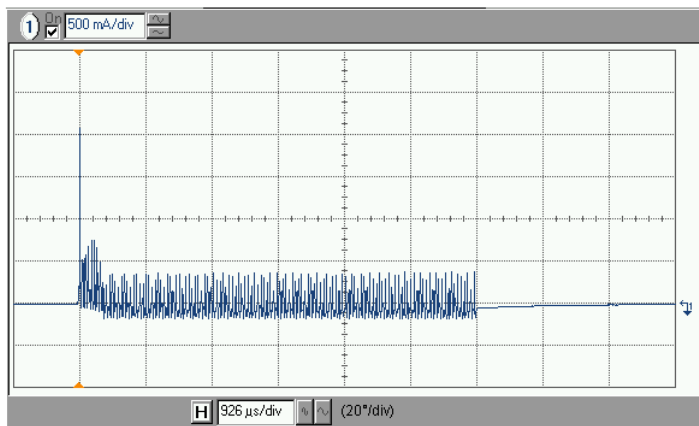


Figure 6. 120° Gate Pulse Profile (Into 1Ω).

<sup>5</sup> Current waveforms obtained using Pearson CT model 2877 (1.0 A/div) with 4 turns terminated with 1.0 MΩ.

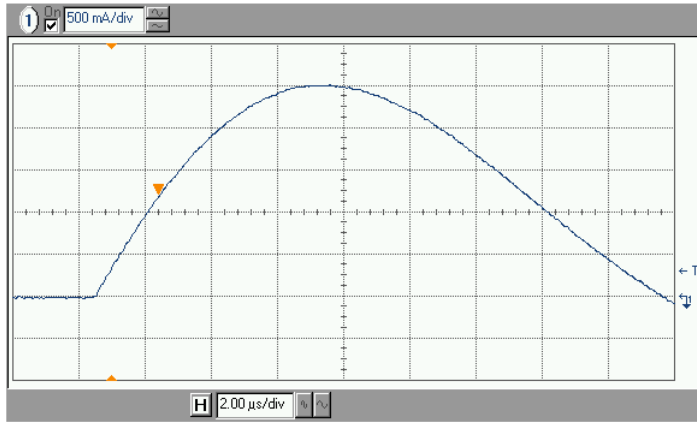


Figure 7. Initial pulse profile detail (Into 1Ω).

The firing circuit uses a phase-locked loop (PLL) circuit locked to the three mains phases. The PLL oscillator output is counted down and decoded into six 120°- wide delayed logic signals. For the 120° single burst profile, the 120°-wide delayed logic signals are modulated by the 23,040 Hz PLL Voltage Controlled Oscillator (VCO) output signal. The two 30°-burst profile is formed by modulating the 120°-wide delayed logic signals with the 23,040 Hz VCO output and the 360 Hz output of a divide-by-64 counter.

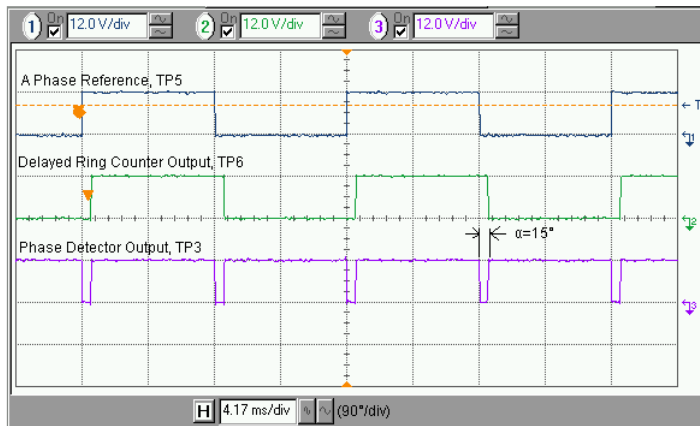


Figure 8. Phase Detector Signals, Phase A:  $\alpha=15^\circ$

- Channels:
1. Phase A Reference, TP5
  2. Delayed Ring Counter Output, TP6
  3. Phase Detector Output, TP3

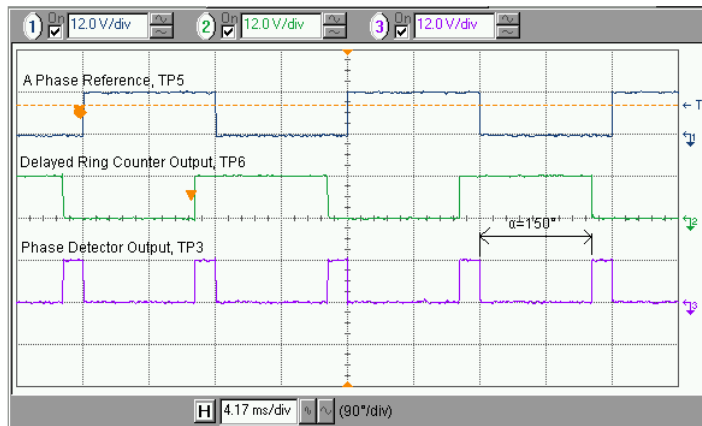


Figure 9. Phase Detector Signals, Phase A:  $\alpha=150^\circ$   
 Channels: 1. Phase A Reference, TP5  
 2. Delayed Ring Counter Output, TP6  
 3. Phase Detector Output, TP3

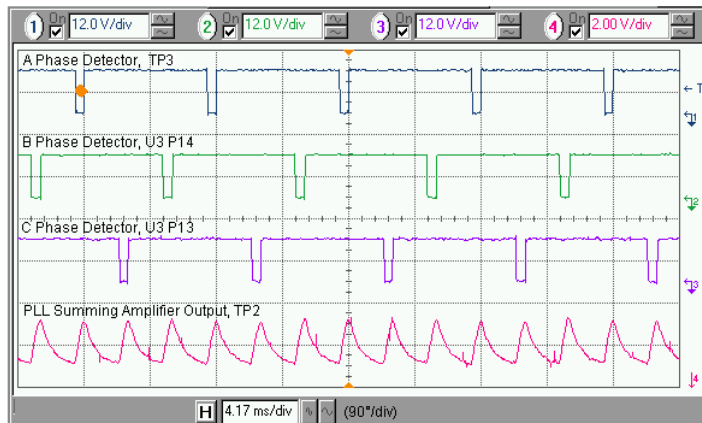


Figure 10. PLL Summing Amplifier Signals:  $\alpha=15^\circ$   
 Channels: 1. A Phase Detector Output, TP3 (U3 P15)  
 2. B Phase Detector Output, U3 P14  
 3. C Phase Detector Output, U3 P13  
 4. Summing Amplifier Output, TP2

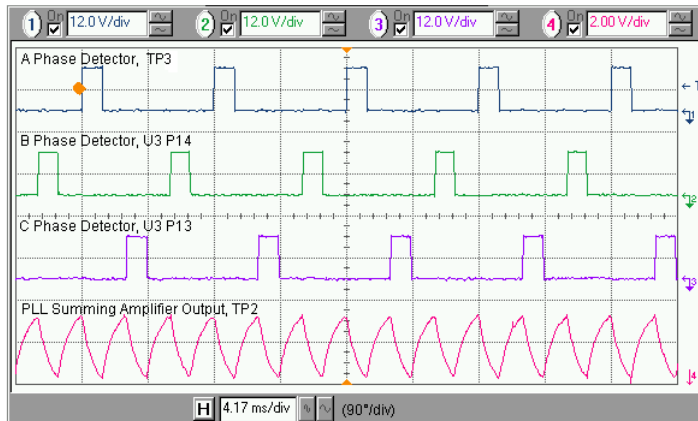


Figure 11. PLL Summing Amplifier Signals:  $\alpha=150^\circ$   
 Channels:      1. A Phase Detector Output, TP3 (U3 P15)  
                   2. B Phase Detector Output, U3 P14  
                   3. C Phase Detector Output, U3 P13  
                   4. Summing Amplifier Output, TP2

## 8.0 GATE PULSE AMPLIFIER

The gate pulse amplifier circuitry shown in E128 revision R consists of the following elements:

- Six IRFD110 MOSFETs (Q1 through Q6), excite the primary of each pulse transformer, driven from the LSI outputs.
- Resistors R3 through R5 and capacitors C2 through C4, which form a gate pulse shaping network.
- Pulse modules PM1 through PM6, which provide current drive for the gate of each SCR. Each pulse module consists of a 2:1 ratio transformer tested for 3500  $V_{RMS}$  isolation, two secondary diodes, noise suppression resistors across the primary and across the gate drive output, and a fusible link in series with the output. Each pulse module is potted in a silicone-based material.

## 9.0 50/60 Hz OPERATION

The FCOG6100 Revision R provides enhanced frequency insensitivity compared to older revisions. A frequency compensation circuit reduces gate drive angle variance with respect to frequency. The gate drive angle decreases by approximately  $5^\circ$  for a 10 Hz decrease in frequency from 60 Hz to 50 Hz. Older configurations exhibited a gate drive angle decrease of approximately  $12.5^\circ$  for the same line frequency change.

For operation with line frequencies in the range of 45 to 60 Hz, no modification to the frequency compensation circuit is required. For

variable-frequency applications, Enerpro's FCOVF6100 provides similar functionality as the FCOG6100, but is tailored for continuous line frequency variations between 30 and 150 Hz.

## 10.0 ELECTRICAL SPECIFICATIONS

The electrical specifications of the General Purpose Firing Board are summarized in the table below. Part numbers refer to drawing E128, revision K.

Table 2. Electrical Specifications.

Characteristic	Performance Requirement	Supporting Information
1. Board-mounted power supply for control electronics and SCR gate drive	24 VA 1 $\Phi$ 50/60 Hz fused board-mounted transformer T1. Center-tapped primary connected for 240V or 480V. 120V/240V or 380V available. Primary connected to mains via SCR cathodes at J2-5,8.	Option 1: For operation on non-standard mains voltage, energize T1 from 120, 240, 380, or 480 Vac through optional connector J4. Option 2: Omit T1 and apply 24Vac or 30VDC to J3.
2. Line voltage reference sensing	Resistive attenuators and 60° phase shift single-pole filters.	Reference signals automatically interchanged for negative phase sequence.
3. Load voltage sensing (optional)	Resistive attenuators provide low level analog of load voltage	Useful for induction motor or generator voltage feedback.
4. PLL reference signal phasing with respect to mains line-to-neutral voltage: a. Reference signals in phase with mains voltage. b. Reference signals lagging mains by 30°	Applications: a. AC controllers with high power factor loads. b. Converters or AC controllers with low power factor loads.	See Section 8.0: Reference Phase Angle Selection.
5. SCR gate waveform. a. Mode 1 b. Mode 2	Pulse profile: a. Two 30° bursts of 32 pulses (23,040 Hz carrier) b. 120° burst of 128 pulses (23,040 Hz carrier)	See Section 9.0: Gate Pulse Profile Selection. a. JU1 Installed b. JU1 Open
6. Gate Delay Command Input	0-5 VDC 0.85-5.85 VDC 0-10 VDC 0-2 VDC 4-20 mA	See Section 4.0: Gate Delay Command
7. Control signal isolation from ground	653 k $\Omega$	Produced by three 2.00 M $\Omega$ mains voltage sense resistors.
8. Gate delay steady-state transfer function	An increase in command voltage produces a proportional decrease in gate delay angle, $\alpha$ .	$\alpha_{max}$ and $\alpha_{min}$ change equally with change in $R_{BIAS}$ (R17). ( $\alpha_{max} - \alpha_{min}$ ) changes with $R_{SPAN}$ (R15).
9. Gate delay dynamic transfer function bandwidth	Attenuation: -3dB at 119 Hz. Phase shift: -45° at 68 Hz	Frequency response may be modified by changing summing amplifier parameters.
10. Gate delay angle balance	Gate pulses for same polarity SCRs are displaced by 120° $\pm$ 1.0°. Gate pulses for opposite polarity SCRs are displaced by 180° $\pm$ 1.0°.	Assumes balanced line-to-line mains voltage. Balance determined by reference comparator offset and attenuation/filter component tolerances.
11. Effect of frequency	$\Delta\alpha/\Delta F = 0.2^\circ/\text{Hz}$ . Improvement over prior versions with active frequency compensation circuit.	See Section 11.0: 50/60 Hz Operation
12. Effect of phase rotation	None.	SCR gating sequence matches mains voltage sequence.
13. Effect of mains voltage distortion.	1. Unaffected by false reference voltage zero crossing. 2. 60° filter attenuates 5 <sup>th</sup> harmonic by 12.8 dB relative to fundamental.	1. No PLL response to short-time false reference logic states. 2. Reference filter attenuates the 5 <sup>th</sup> , 7 <sup>th</sup> , 11 <sup>th</sup> , etc harmonics from 6-pulse SCR switching.
14. Lock acquisition time	Approximately 30 ms.	Gating is inhibited for 20 ms or longer at

		power-on. Inhibit period depends on soft-start time constant.
15. Soft-start	Gating commences at $\alpha_{max}$ and exponentially decays to the commanded delay when $\overline{I_2}$ is ungrounded (J3-12).	Soft-start time constant is set by soft-start timing resistor and capacitor.
16. Soft-stop	Gate-delay angle ramps to $\alpha_{MAX}$ before being inhibited by grounding $\overline{I_2}$ .	Soft-stop time constant is set by soft-stop timing resistor and capacitor
17. Phase loss inhibit	Loss of a mains voltage or severe phase unbalance causes gate inhibit.	Gating resumes with $\alpha = \alpha_{MAX}$ . Ramps to commanded delay angle as determined by soft-start time constant. Circuit operation is immune to line frequency variations and SIG HI transients.
18. Power-on inhibit	Phase loss inhibit circuit is activated at power-on.	Same delay angle response as with phase loss inhibit.
19. Instantaneous inhibit	Opening the connection of $\overline{I_1}$ to +12VDC instantly inhibit SCR gating. Closing this connection instantly enables SCR gating.	Gating is inhibited if P3 is removed.
20. SCR gate current individual pulse width	$T_{ON}$ and $T_{OFF}$ vary from 15 $\mu$ s to 28 $\mu$ s.	Gate current ON and OFF time vary with gate delay angle due to 360 Hz FM in the VCO output.
21. Peak gate drive open circuit voltage	15 V	Supply voltage = 30 VDC
22. Peak gate drive short circuit current	2.0 A	Measured with 30 VDC supply and 1.0 $\Omega$ load resistor.
23. Gate drive current rise time (short circuit)	0.5 A in 0.5 $\mu$ s	Measured with 30 VDC supply and 1.0 $\Omega$ load resistor.
24. Ambient temperature	0° - 65° C	Forced air cooling required for ambient temperatures > 65° C

## 11.0 INSTALLATION AND CHECKOUT

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCR unit. An EP1032A transformer (240V/480Vac) T1 is assumed.

**11.1.** Ensure that the power is off. Wire a plug, P2, with mains voltage connected to sockets 2, 5, and 8. Insert plug P2 into header J2.

**11.2.** If the FCOG6100 board is set up to obtain board power from the SCR cathodes proceed to step 12.3. If not, connect the appropriate power to J4; J4-1 and J4-5 for 480Vac or J4-3 and J4-5 for 240Vac board power.

**11.3.** Install plug P3 with the 0/5Vdc delay command signal, signal common, and inhibit contact closure leads wired to the plug.

**11.4.** Energize the mains voltage; this will energize the FCOG6100 board. (Alternatively, energize the mains voltage and then energize the FCOG6100 by 120 Vac, 24 Vac, 30 VDC, or as specified).

**11.5.** Verify the presence of regulated +12 VDC  $\pm$  5% at J3-6 and regulated +5 VDC  $\pm$ 5% at J3-7 with a multimeter.

**11.6.** Verify that the PLL is in lock and the mains voltages are balanced by noting the Phase Loss LED is not lit.

**11.7.** Verify that the DC level of the VCO control voltage at TP2 is approximately 5.0 VDC. This voltage is factory-set by selection of the VCO timing select resistor.

**11.8.** Determine the PLL gate delay angle from the pulse width of the A-phase detector output at TP3: Calibrate the oscilloscope time-base at 20°/div (0.926 ms/div at 60 Hz). Read the gate delay angle directly from the TP3 pulse off time.

**11.9.** Vary the delay command voltage from 0 VDC to 5.0 VDC. Observe that the gate delay angle at TP3 has the desired minimum and maximum values.

**11.10.** To increase the minimum and maximum gate delay angles by an equal amount, increase the value of the delay bias resistor, R17. To increase the difference between the maximum and minimum delay angles, reduce the value of the delay span resistor, R15.

<b>Document Revision History</b>			
<b>Revision</b>	<b>Date</b>	<b>Notes</b>	<b>Approval</b>
NC	06/2008	Initial release	JTM
A	12/2009	Correct SIG HI values in Table 1	JTM