

**OPERATING MANUAL FOR A 6-SCR GENERAL PURPOSE
GATE FIRING BOARD, PART NO. FCOG6100 REV. J, J', J'', K****INTRODUCTION**

This manual is intended to familiarize the user with the salient features and specifications of the firing board. A simple checkout procedure is included together with typical firing circuit signal waveforms.

PRODUCT DESCRIPTION**APPLICATION**

The general purpose firing board responds to a voltage or milliamp current signal to produce a delayed set of six 60° spaced high current SCR gate pulses. A programming plug adapts the board to suit various types of SCR controllers or converters (rectifiers). The range of applications is further enhanced by the use of Auxiliary Firing Board's. These board's extend the usage to the gating of:

- paralleled SCRs
- twelve-pulse converters¹
- four-quadrant converters
- sequence reversing controllers
- remote operation of SCR's

An optional mode transition gate inhibit circuit can be installed for use with four-quadrant converters and sequence reversing controllers.

LSI LOGIC DEVICE

All of the firing circuit logic is contained in a custom 40-pin CMOS LSI gate array. Additional detail on the firing circuit theory is contained in an engineering society paper.²

BOARD MOUNTED CONNECTORS

The firing board is completely connectorized to simplify maintenance and trouble shooting.

¹ For use in 12-pulse applications please contact ENERPRO. We manufacture boards specifically for this application.

² Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.

Gate/Cathode Connectors

The SCR gate/cathode interface is provided by 8-position Mate-N-Lok™ right angle headers³, J1 and J2, and mating plugs, P1 and P2. The jacks are keyed to prevent incorrect installation of the mating plugs. Plug P1 accesses the gates and cathodes of the three SCRs having load connected cathodes when the SCRs are arranged in the in-line ac controller or bridge converter configurations. Similarly, plug P2 accesses the gates and cathodes of the three SCRs having line connected cathodes.

Plug P1 or P2 and the associated cable are omitted when the firing board is used with 3 SCR/3 diode circuits.

Control Signal Connector

The firing board is connected to the gate delay command and inhibit controls through a 12-position Mate-N-Lok™ connector designated as J3. This connector also accesses the outputs of the 24Vac board mounted transformer, the 30Vdc rectifier, the regulated +12Vdc and the regulated +5Vdc output's. The 24Vac and 30Vdc connections permit the board to be powered from an external source. With the board mounted transformer installed, approximately 10 watts of ac or dc power is available from J3 to power lamps or a control relay.

Optional Power Supply Excitation

The board mounted 24VA power supply transformer is normally energized by connection with insulated wire to two of the mains voltages which appear at positions 5 and 8 of header J2. When the SCRs are powered from non-standard voltages, the board mounted power supply transformer can be energized through the optional 5-position Mate-N-Lok™ plug/header, P4/J4.

Optional Reference Connector

In certain applications, the ac mains voltage may not be present at the SCR cathodes or the ac voltage may go to zero during load faults⁴. In these cases, or when galvanic isolation is required between power and control circuits, external reference voltages are applied through optional Mate-N-Lok™ plug P5. The mating header, J5, and voltage sensing resistors R37, R38 and R39 are installed on the board space normally occupied by power supply transformer T1. Board power is then obtained externally from 24Vac or 30Vdc applied through P3/J3.

Test Signal Input Connector

A 3-position cable header, J7A, is used to inject low level 3-phase test reference signals from a firing board test fixture into the delay generator circuit. This allows the board checkout to proceed without connection to high voltage power.

In addition a three position Mate-N-Lok™ connector, J7B, is available for this purpose or for connection of externally attenuated phase reference signals. The

³ Vertical headers are available upon request.

⁴ For example, in a 6-SCR interphase transformer converter or an arc welder converter.

use of J7B and external attenuating resistors allows the use of the onboard transformer while still providing connection to external phase references.

Auxiliary Regulator Board Connector

Key firing board signals are brought out to a 20-position ribbon cable connector socket, J6, for interfacing with a second printed circuit board which can be conveniently mounted on stand-offs above the firing board. This regulator board can provide various closed-loop functions (torque, speed, position voltage, power, etc.) and diagnostic circuitry. The 20-position connector socket also facilitates board testing.

Auxiliary Firing Board Connector

Two 8-position cable headers, J8 and J9, are provided to connect either of two sets of six gate command logic signals, as well as 30Vdc power and common, to the FCOAUX60 Auxiliary Firing Board for gating an additional set of six SCRs (the FCOAUX60 can be ganged if additional SCRs are required) in parallel⁵ with the primary set of SCRs (using J8), or for any of the applications described under Bipolar Firing options (using J9).

Two-quadrant 12-pulse gating⁶ may be achieved, with the FCOAUX60 connected to J9, by connecting the P logic signal (J6-19) to the 360Hz clock, CK2 (J6-4); changing RN5 to a 6-pin SIP; replacing R64 with a wire jumper and cutting the trace from P to the +12V at the point indicated on the board.

Frequency Selection Connector

A 3-position header, J10, is used in conjunction with RN2⁷ to select between 50Hz and 60Hz operation. In 60Hz operation RN2 is 120k and R47 is connected in parallel with R46. In 50Hz operation RN2 is 150k and J10 removes R47 from the circuit in order to maintain TP2 at 5.0Vdc.

GATE DELAY COMMAND

The gate delay command signal, SIG HI, may be a zero to 5.0Vdc voltage signal or a current signal with an upper limit of 50mA. The input resistance presented to the delay command signal is determined by resistor R41, connected in shunt with the control signal input. The value of R41 is selected at 10 k when the control signal is a voltage source. As an option, a 0.9Vdc to 5.9Vdc input signal may be used by changing R52 to 249 k . When the gate delay command is a current signal, R41 is selected to give a 5.0Vdc level at the maximum delay command signal current.

GATE INHIBITS

⁵ The FCOREM60 Auxiliary Firing Board is designed to provide high output gate pulses in order to increase the reliability of firing in parallel applications. The FCOREM60 board uses the gate signal outputs from PM1 through PM6.

⁶ For use in 12-pulse applications please contact ENERPRO. We manufacture boards specifically for this application.

⁷ RN2 may be placed in a socket for ease of modification.

SCR gating is inhibited by making either or both of the inhibit signal points, designated as I1 and I2 and appearing at pins 4 and 12 of J3, a logic zero.

In the case of the instantaneous inhibit, I1, resistor RN5-4,3 on the firing board is provided to pull the I1 signal point low if the connection between I1 and +12Vdc is opened. This ensures that SCR gating is inhibited if plug P3 is inadvertently disconnected. In applications where the instantaneous gate inhibit function is not utilized, a jumper wire is installed between pins 4 and 6 of P3 to hold I1 at +12Vdc when P3 is installed in J3.

The inhibit signal I2 is connected to +12Vdc through pull-up resistor RN-5,6 on the firing board. When I2 is grounded, the gate delay angle is ramped to the maximum delay angle before gating is inhibited. This is termed the "Soft-Stop" shutdown mode. Removing the ground on I2 causes gating to be enabled with the delay angle set to the maximum limit. The delay angle then ramps down to the commanded angle. This is termed the "Soft-Start" turn-on mode. The Soft-Stop and Soft-Start periods are determined by timing resistors R45 and R44, and capacitor C3.⁸

PHASE-LOSS INHIBIT

A phase loss circuit operates to instantly inhibit SCR gating if the mains phase balance is abnormal or, in the extreme case, if one phase voltage is missing. Gating is enabled when the proper phase balance is restored: gating initiates at the maximum delay angle, and ramps down to the commanded angle at a rate determined by the Soft-Start RC time constant.

The phase-loss inhibit circuit is also activated when three phase power is initially applied to the SCRs. Gating is inhibited until the power supply voltage has stabilized. Gating then commences at the delay angle limit and ramps down to the commanded angle at a rate determined by the Soft-Start RC time constant.

BIPOLAR FIRING OPTIONS

Two-quadrant six-pulse is provided by the FCOG6100 Firing Board. The FCOAUX60 Auxiliary Firing Board extends the application to two-quadrant 12-pulse, four-quadrant six-pulse and sequence reversing 12-SCR ac controllers. An optional mode transition timed gate inhibit is provided for four-quadrant converters and sequence reversing controllers.

A logic one P signal from an active low signal source applied to position 5 of connector J3 enables the gate drive from the main firing board and inhibits the gating from the auxiliary firing board. A logic zero P signal inhibits the main board and enables the auxiliary board.

When the P signal is toggled by the 360 Hz clock the FCOG6100 is set-up to deliver a 120° pulse. This 120° burst is then cut up to allow both firing boards to provide two 30°-wide bursts of 23,040 Hz gate pulses spaced by 30°. The six

⁸ See electrical specifications table for formula's.

gate outputs from the auxiliary board are delayed by 30° from the corresponding gate outputs from the main firing board, as required for 12-pulse gating.

Four-Quadrant 3-Pulse Converter

Four-quadrant 3-pulse gating from the FCOG6100 firing board is achieved by grounding the T signal (U4-28) at the point indicated on the board. The gate drive to the positively poled SCRs is then provided by pulse modules PM1 through PM3, and to the negatively poled SCRs by PM4 through PM6. The optional polarity transition gate inhibit circuit, consisting of U9, RN6, C29, C30, and R65, inhibits gating for approximately 100 msec at each transition of the polarity command signal P.

Four-Quadrant 6-Pulse Converter

Four-quadrant 6-pulse gating is obtained from the main firing board and auxiliary firing board by connecting the 8-conductor inter-board cable to J9 on the main firing board. Positively poled SCRs are then gated by the main firing board, negatively poled SCRs by the auxiliary firing board. The optional polarity transition gate inhibit circuit, consisting of U9, RN6, C29, C30, and R65, inhibits gating for approximately 100 msec at each transition of the polarity command signal P.

Two-Quadrant 12-Pulse Converter

Two-quadrant 12-pulse gating is provided with the inter-board cable from the auxiliary firing board connected to J9 on the main firing board and:

- Placing a jumper between pins 4 and 19 of J6 to connect the 360 Hz clock to the P logic signal,
- Changing RN5 to a 6-pin SIP network,
- Replacing R64 with a jumper wire,
- Cutting the trace from P +12V at the point indicated on the board.

REFERENCE PHASE ANGLE SELECTION

A programming plug PP1 is installed to select phase reference logic signals which are either in-phase with, or 30° lagging, the mains line-to-neutral voltage. In-phase references (PP1 positions 1, 2, and 3 open: positions 4, 5, and 6 closed) serve for phase delay control of in-line antiparallel pairs of SCRs (AC controllers). 30° lagging references (PP1 positions 1, 2, and 3 closed: positions 4, 5, and 6 open) are used with SCR rectifiers (converters).

GATE PULSE PROFILE SELECTION

The programming plug PP1 also serves to select one of three SCR gate current pulse patterns:

1. One 120°-wide burst of 23,040 Hz carrier.
2. Two 30°-wide bursts of 23,040 Hz carrier spaced by 30°.
3. Two single pulses spaced by 60°

The firing circuit uses a phase-locked loop(PLL) circuit locked to the three mains phases. The PLL oscillator output is counted down and decoded into six 120°-wide delayed logic signals. In pulse pattern #1 above, the 120°-wide delayed

logic signals are modulated by the 23,040 Hz PLL Voltage Controlled Oscillator (VCO) output signal. The double burst pattern #2 above is formed by modulating the 120°-wide delayed logic signals with the 23,040 Hz VCO output and the 360 Hz output of a divide-by-64 counter. Pulse pattern #3 is obtained by modulating the 120°-wide delayed logic signals with 360 Hz to form two transformers. The transformers saturate after approximately 100 μ s but this is of no consequence because of the current limiting resistor in series with each of the transformer primary windings.

GATE PULSE AMPLIFIER

Circuitry shown in E128 consisting of transistor array U3, resistors R3 through R6, capacitors C11 through C13, and gate pulse isolation modules PM1 through PM6 amplify and shape the thyristor gate current pulses. Each pulse module consists of a 2:1 ratio pulse transformer tested for 3500Vrms isolation, two secondary diodes, noise suppression resistors across the primary and across the gate drive output, and a fuse in series with the output.

ELECTRICAL SPECIFICATIONS

The electrical specifications of the General Purpose Firing Board are summarized in the table below. Part numbers refer to drawing E128, rev. K.

Characteristic	Performance Requirement.	Supporting. Information
1. Board mounted power supply for control electronics and SCR gate drive.	24VA 1 \emptyset 50/60 Hz fused board mounted transformer T1. Center-tapped primary connected for 240V or 480V. 120V/240V or 380V avail. Primary connected to mains via SCR cathodes at J2-5,8.	Option 1: For operation on non-standard mains voltage, energize T1 from 120V, 240V, 380V, or 480V through optional connector J4. Option 2: Omit T1 and apply 24Vac or 30Vdc to J3.
2. Line voltage reference sensing	Resistive attenuators and 60° phase shift single pole filters.	Reference signals automatically interchanged for negative phase sequence.
3. Load voltage sensing(optional).	Resistive attenuators produce low level replica of load voltage.	Useful for load voltage feedback control.
4. PLL reference signal. phasing w.r.t. mains line-to-neutral voltage: a. ref. signals in phase with mains voltage. b. ref. signals lagging mains voltage by 30°.	Application: a. AC controllers with high power factor loads. b. Converters of AC controllers with low power factor loads.	PP1 programming plug: a. #1,2,3 open #4,5,6 closed b. #1,2,3 closed #4,5,6 open
5. SCR gate waveform. a. Mode 1 b. Mode 2 c. Mode 3	Pulse Profile: 120° burst of 128 pulses(23,040 Hz carrier) two 30° bursts of 32 pulses(23,040 Hz carrier) two single 60° spaced pulses, 100 μ s wide.	PP1 programming plug: #7 open #8 closed #7 closed #8 closed #7 closed #8 open
6. Input control signal.	0 Vdc to 5.0Vdc control signal. Load resistance is 8.33 K .	Option 1: 0.9 Vdc to 5.9Vdc control signal. Option 2: a Shunt resistance (R41) across signal input can be selected for milliamp control signal.
7. Control signal isolation from ground.	653 K	Produced by the three 2.00 M mains voltage sense resistors, R31-33.

8. Gate delay steady-state transfer function.	Increase in command voltage produces a proportional decrease in gate delay angle, θ .	θ_{max} and θ_{min} change equally with change in R_{bias} (R43). ($\theta_{max} - \theta_{min}$) changes with R_{span} (R42).
9. Gate delay dynamic transfer function bandwidth.	Attenuation = -3dB at 119Hz. Phase shift = -45° @ 68Hz.	Frequency response can be modified by changing summing amplifier parameters.
10. Gate delay angle balance.	Gate pulses for same polarity SCRs are displaced by $120^\circ \pm 1.0^\circ$. Gate pulses for opposite polarity SCRs are displaced by $180^\circ \pm 1.0^\circ$.	Assumes balanced line-to-line mains voltage. Balance determined by reference comparator offset and attenuator/filter component tolerances.
11. Effect of frequency.	$Da/Df = 1.5^\circ/Hz$. For 50 Hz operation, compensate by removing R47 and changing RN2 to 150K.	Due to Type I PLL and 60° phase shift low pass reference filters.
12. Effect of phase rotation.	none	SCR gating sequence matches mains voltage sequence.
13. Effect of mains voltage distortion.	1) unaffected by false reference voltage zero crossing. 2) 60° filter attenuates 5th harmonic by 12.8dB relative to fundamental.	1) No PLL response to short-time false reference logic states. 2) Reference filter attenuates the 5th, 7th, 11th, etc. harmonics from 6-pulse SCR switching.
14. Lock acquisition time.	Approximately 29ms.	Gating is inhibited for 20ms or longer at power-on. Inhibit period depends on Soft-Start time constant.
15. Soft-Start	Gating commences at θ_{max} and exponentially decays to the commanded delay when $\langle I_2 \rangle$ is ungrounded(J3-12).	Soft-Start time constant is set by C3 and R44. $T = (1.5k + R44)(C3)(0.579)$ T = mSec, R = k, C = μF R44 20.0k
16. Soft-Stop	Gate-delay angle ramps to θ_{max} before being inhibited when $\langle I_2 \rangle$ is grounded.	Soft-Stop time constant is set by C3 and R45. $T = R45(C3)(1.84)$ T = mSec, R = k, C = μF R45 1.0k
17. Phase loss inhibit.	Loss of a mains voltage or severe phase unbalance causes gate inhibit.	Gating resumes with $\theta = \theta_{max}$. θ ramps to commanded delay angle as determined by Soft-Start time constant.
18. Power-on inhibit.	Phase loss inhibit circuit is activated at power-on.	Same delay angle response as with phase loss inhibit.

19. Instantaneous inhibit.	Opening the connection of <l1>(P3-4 or P6-8) to +12V instantly inhibits SCR gating. Closing the connection of <l1> to +12V instantly enables SCR gating.	Gating is inhibited if P3 is removed.
20. SCR gate current individual pulse width.	T _{on} and T _{off} vary from 15μs to 28μs.	Gate current ON and OFF times vary with gate delay angle because of 360Hz FM in the VCO output.
21. Peak gate drive open circuit voltage	15V	With a 30Vdc supply voltage
22. Peak gate drive short circuit current.	2.0A	Measured with a 30Vdc supply voltage and a 1.0 load resistor
23. Gate drive current risetime(short circuit)	.5A in .5μs	Measured with a 30Vdc supply voltage and a 1.0 load resistor
24. Ambient temperature.	0°C to 70°C	

INSTALLATION AND CHECKOUT

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCR unit. An EP1032A transformer (240V/480Vac) T1 is assumed.

1. Ensure that the power is off! Wire a plug, P2, with mains voltage connected to sockets 2, 5, and 8. Insert plug P2 into header J2.
2. If the FCOG6100 board is set-up to obtain board power from the SCR cathodes proceed to step 3. If not, connect the appropriate power to J4; J4-1 and J4-5 for 480Vac or J4-3 and J4-5 for 240Vac board power.
3. Install plug P3 with the 0/5Vdc delay command signal, signal common, and inhibit contact closure leads wired to the plug.
4. Energize the mains voltage, this will energize the FCOG6100 board.
5. Verify the presence of regulated +12Vdc \pm 5% at J3-6 and regulated +5Vdc \pm 5% at J3-7.
6. Verify that the PLL is in lock by noting the response of the A-phase detector output at TP3 to a change in the delay command signal voltage applied to pins 10 and 11 of J3.
7. Verify that the DC level of the VCO control voltage at TP2 is approximately 5.0Vdc. This voltage is factory set by selection of R46.
8. Determine the PLL gate delay angle from the pulse width of the A-phase detector output at TP3: Calibrate the oscilloscope timebase at 20°/div. Read the gate delay angle directly from the TP3 pulse off time.
9. Vary the delay command voltage from 0Vdc to 5.0Vdc. Observe that the gate delay angle at TP3 has the desired minimum and maximum values.
10. To increase the minimum and maximum gate delay angles by an equal amount, increase the value of the delay bias resistor, R43. To increase the difference between the maximum and minimum delay angles, reduce the value of the delay span resistor, R42.

FIRING BOARD WAVEFORMS

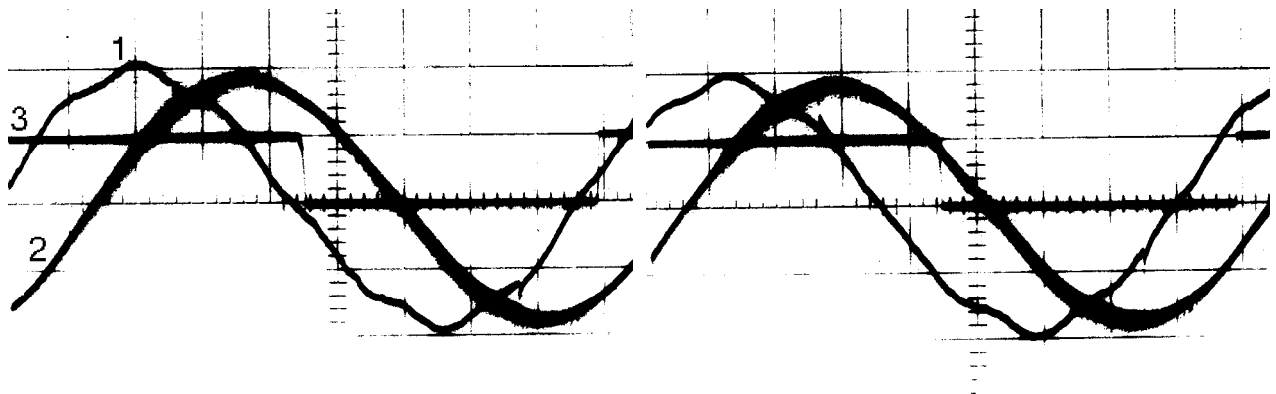
The following waveforms were obtained with the firing board connected to 240 Vac 60 Hz balanced 3-phase power via sockets 2, 5, and 8 of plug P2. All logic signals are shown with a scale factor of 10 V/div. The time (X) axis scale factor is $40^\circ/\text{div}$ unless otherwise noted. Component designations U7 etc. refer to drawing number E128, Rev. K. Component pins are designated U7-1, etc.

A. Mains Voltage Signals, A phase.

Trace: 1. Line to neutral mains voltage, 150 V/div
 2. Attenuated and filtered mains voltage at RN2-5, .2 V/div
 3. Reference comparator output at TP5, U7-1

a. 0° references

b. -30° references

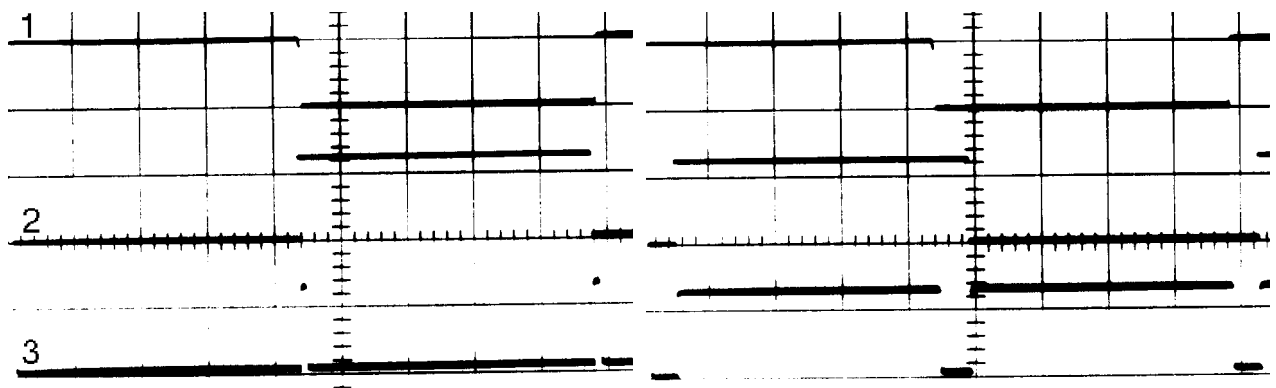


B. Phase Detector Signals, A phase.

Trace: 1. A-phase reference at TP5 (U7-1).
 2. Delayed ring counter output at TP6 (U4-26)
 3. Phase detector output at TP3 (U4-22).

a. $= 175^\circ$

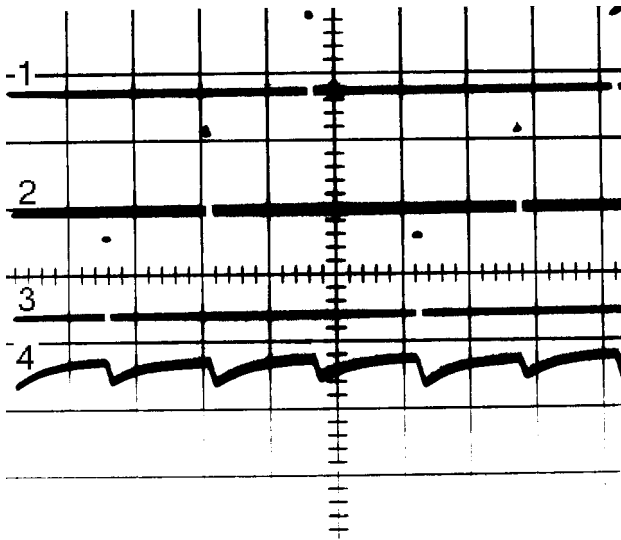
b. $= 18^\circ$



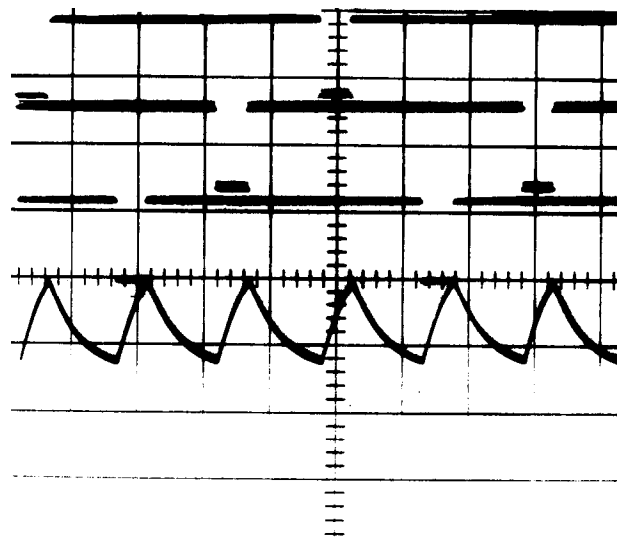
C. PLL Summing Amplifier Signals

- Trace:
1. A phase detector output at U4-22 (TP3)
 2. B phase detector output at U4-21
 3. C phase detector output at U4-20
 4. Summing amplifier output at U6-8 (TP2), 2 V/div.

a. $= 175^\circ$



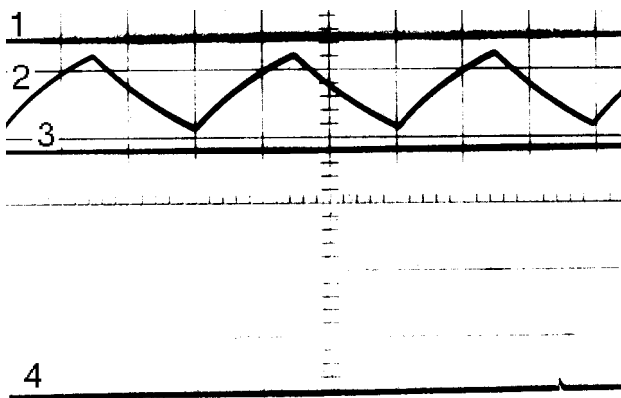
b. $= 18^\circ$



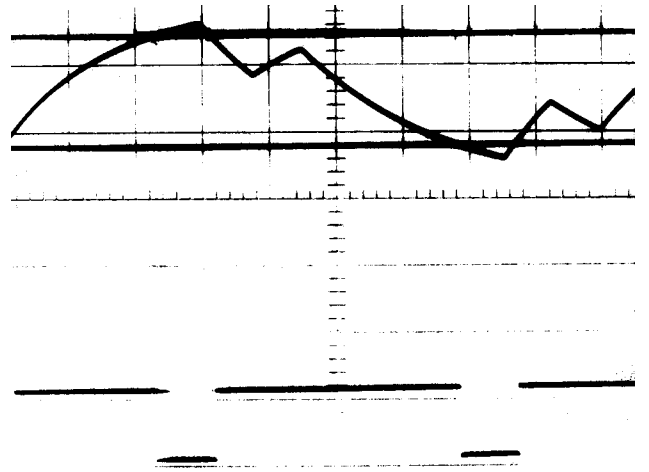
D. Phase Loss Comparator Signals

- Trace:
1. Upper threshold voltage at U5-7
 2. Summed and filtered A-B-C reference signal at U5-5 (TP8)
 3. Lower threshold at U5-4
 4. comparator output at U5-1 (\overline{PL} logic signal)

a. normal operation

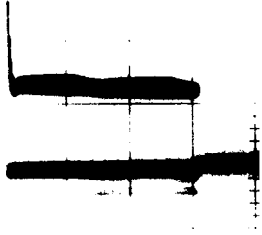


b. one mains phase missing

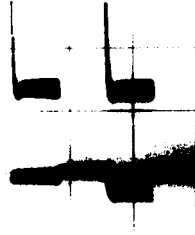


E. Pulse Transformer Output into 1.0 load (.5 A/div)

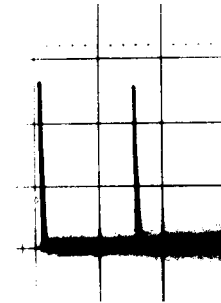
1. 120° burst of 23kHz



2. Two 30° bursts



3. Two isolated pulses



4. Initial pulse detail (.5 A/div, 2 μs/div)

