

PART	DESCRIPTION
U1	W02M
U2	LM340LAH-12
U3	ULN2004A
U4	EP1011A
U5	LM239N
U6	LM224N
U7	LM224N
U8	MC14053BCP
U9	MC14077BCP (16)
DN1	MAD1109P
RN1	MDP1403153G
RN2	MSP08A03124G
RN3	MSP08A03473G
RN4	MSP08A01104G
RN5	MSP08A03152G
RN6	MSP08A03154G (16)
CR1-CR2	1N4746A(18V)/1N5241B(11V)
CP1-CP2	PCB-2
PP1	435704-8
J1-J2/P1-P2	640584-1/640582-1
J3/P3	350433-1/1-480708-0
J4/P4	1-350945/350809-1
J5/P5	1-350949-0/1-480763-0
P1-P5 SOCKETS	350689-3 (24-18AWG)
J6/P6	103311-5/499568-4
J7A/P7A	640454-3/640440-3
J7B/P7B	350789-1/350766-1(optional)
J8/P8	640456-8/640440-8
J9/P9	640456-8/640440-8
J10/P10	640454-3/65474-001
C1-C2	470µF 50V ECEA1HV471S
C3	22µF 16V ECSF16E22
C4 -C5	2.2µF 16V ECSF16E2R2
C11-C13	MKC4 10% 63V
C21-C28	MKS3 5% 63V/100V
C31-C33	FKC3 5% 160V
C34	MKS02 20% 50V
C35	MKS3 5% 63V
R1	CW2C 300 5%
R2	CW2C (8) 5%
R3	CW2C 10 5%
R4-R6	CW5 200 5%
R31-R39	1/2 W 2.00M 1% RN65D2004F
R41-R67	1/4 W 1% RN60
PD1-PD2/PD3	550-2404 (RED)/550-2204(GRN)
T1	EP1030(120), EP1031(120/240)
T1	EP1032A(240/480) EP1031-1(240)
T1	EP1033B(350)
PM1-PM6	EP1019C'

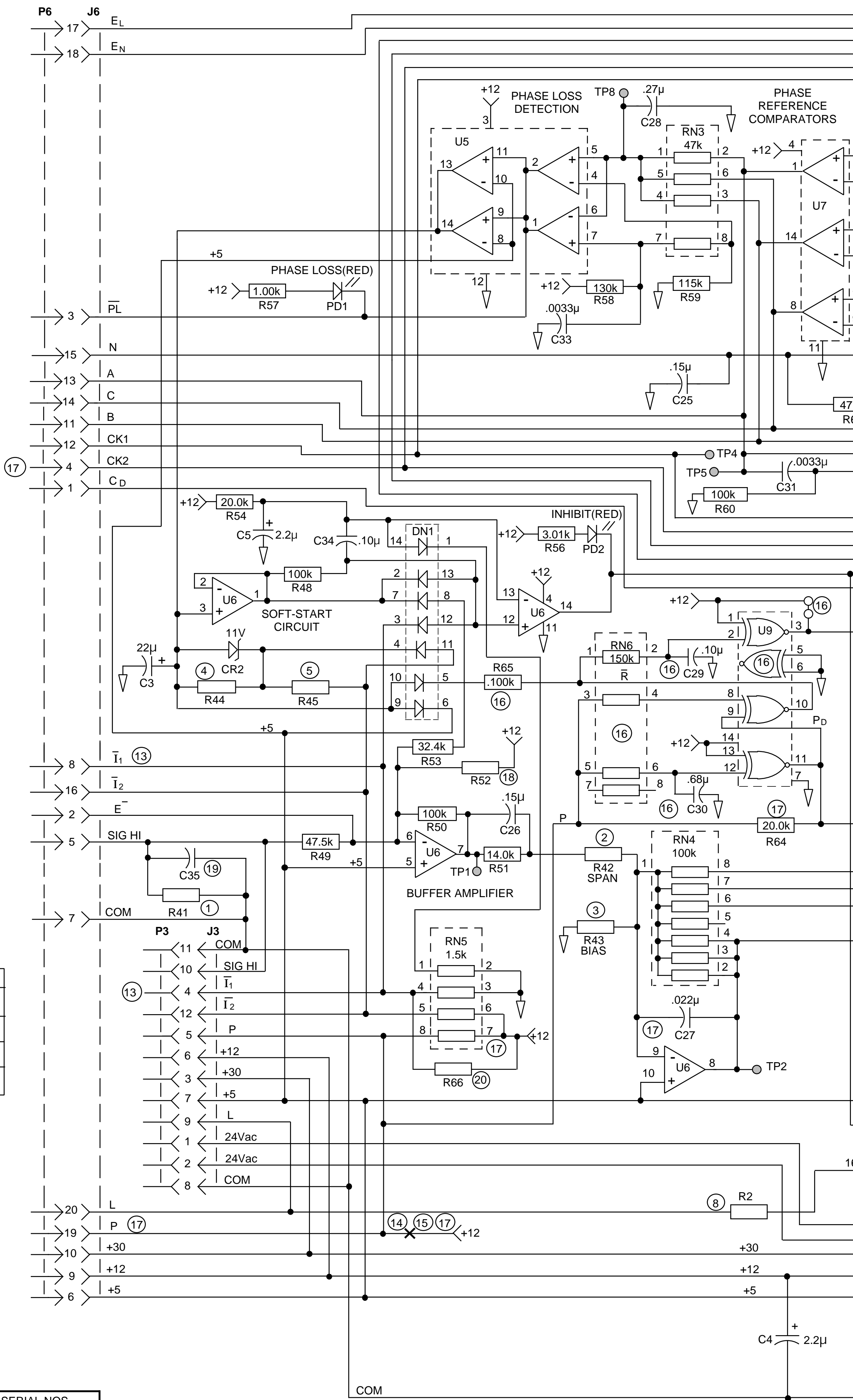
NOTES

- For current signal input select R41 to give SIG HI = +5.0 Vdc with maximum signal current.
- Select R42 for desired gate delay span. } consult factory for recommended delay angle limits for a specific application
- Select R43 for desired gate delay bias. }
- Select R44 for desired soft-start time.
- Select R45 for desired soft-stop time.
- Factory selected R46.
- For 50 Hz, install P10 in positions 2 and 3 and change RN2 to 150k
- Select R2 resistance for +24V control voltage.
 - U3-16 = +30 when gating is inhibited
 - U3-16 = +.5 when gating is enabled(typical voltages)
- Select PP1 shunts as shown in dwg. E128, sheet 1.
- For off-board phase references:
 - install R37-R39 and J5.
 - omit R31-R33 and T1.
- J7 provided for test reference inputs(J7A) or mains voltage output signals(J7B).
- For gating paralleled SCRs connect FCOAUX60 auxiliary board via cable to J8.
- Make +12V connections to J3-4 or to J6-8 to instantly enable SCR gating. The inhibit signal is gated by CK1 to prevent randomly narrow gate pulses
- For four-quadrant six-pulse gating:
 - cut +12V trace to J6-19 and J3-5 labelled "Cut Trace for Bipolar Operation."
 - connect P to +12V to enable "A" bridge.
 - connect P to COM to enable "B" bridge.
 - connect FCOAUX60 board via cable to J9.
- For four-quadrant three-pulse gating:
 - cut +12V trace to J3-5 and J6-19 labelled "Cut Trace for Bipolar Operation."
 - connect jumper JU1 from U4-28 to COM.
 - connect P to +12V to enable +A, +B, +C SCRs.
 - connect P to COM to enable -A, -B, -C SCRs.
- For four quadrant polarity transition inhibit:
 - install U9, RN6, C29, C30 and R65.
 - cut trace from U9-3 to +12V labelled "Cut Trace for Polarity Transition Inhibit."
- For two-quadrant 12-pulse gating:
 - cut +12V trace to J3-5 and J6-19 labelled "Cut Trace for Bipolar Operation."
 - connect jumper from J6-4 to J6-19.
 - change RN5 to 6-pin SIP network.
 - make C27 = .047µF, replace R64 with jumper.
 - connect FCOAUX60 board via cable to J9.
 - open PP1 position 7, close position 8.
- R52 = 150k for 0V < SIG HI < 5.0V
R52 = 249k for .9V < SIG HI < 5.9V
- Optional capacitor C35 to reduce the bandwidth of the firing circuit
- Optional 1.50k pullup resistor R66, connect I1 to COM for instant inhibit.
- Install jumper JU4 to +12 when using the 2-60 degree spaced gate pulse profile.
- Optional speed-up values: C26 = .068µ, C27 = .0022µ, R51 = 28.0k, R42 = R42' - 14.0k where R42' = standard value of R42.

RN60 RESISTORS (k) (22)				MK/FK CAPACITORS(µF) (22)			
R41	NOTE 1	R55	3.01	C11	.33	C31	.0033
R42	NOTE 2	R56	3.01	C12	.33	C32	.00068
R43	NOTE 3	R57	1.00	C13	.33	C33	.0033
R44	NOTE 4	R58	130	C21	.033	C34	.10
R45	NOTE 5	R59	115	C22	.033	C35	(19)
R46	NOTE 6	R60	100	C23	.033		
R47	115	R61	47.5	C24	.033		
R48	100	R62	14.0	C25	.15		
R49	47.5	R63	10.0	C26	.15		
R50	100	R64	20.0	C27	.022		
R51	14.0	R65	.100(16)	C28	.27		
R52	NOTE 18	R66	NOTE 20	C29	.10 (16)		
R53	32.4	R67	2.00	C30	.68 (16)		
R54	20.0						

Rev. K

		ENERPRO	
		GENERAL PURPOSE 3Ø FIRING CIRCUIT	
dwn:	fjb	6-6-89	
chkd	web	6-14-89	
rev:	fjb	8-30-89	
VERSION	12-18-91		
		PCB PN FCOG6100	Dwg. No. E128
		Sheet 2 of 2	



PP1 PHASE REFERENCE SELECTION

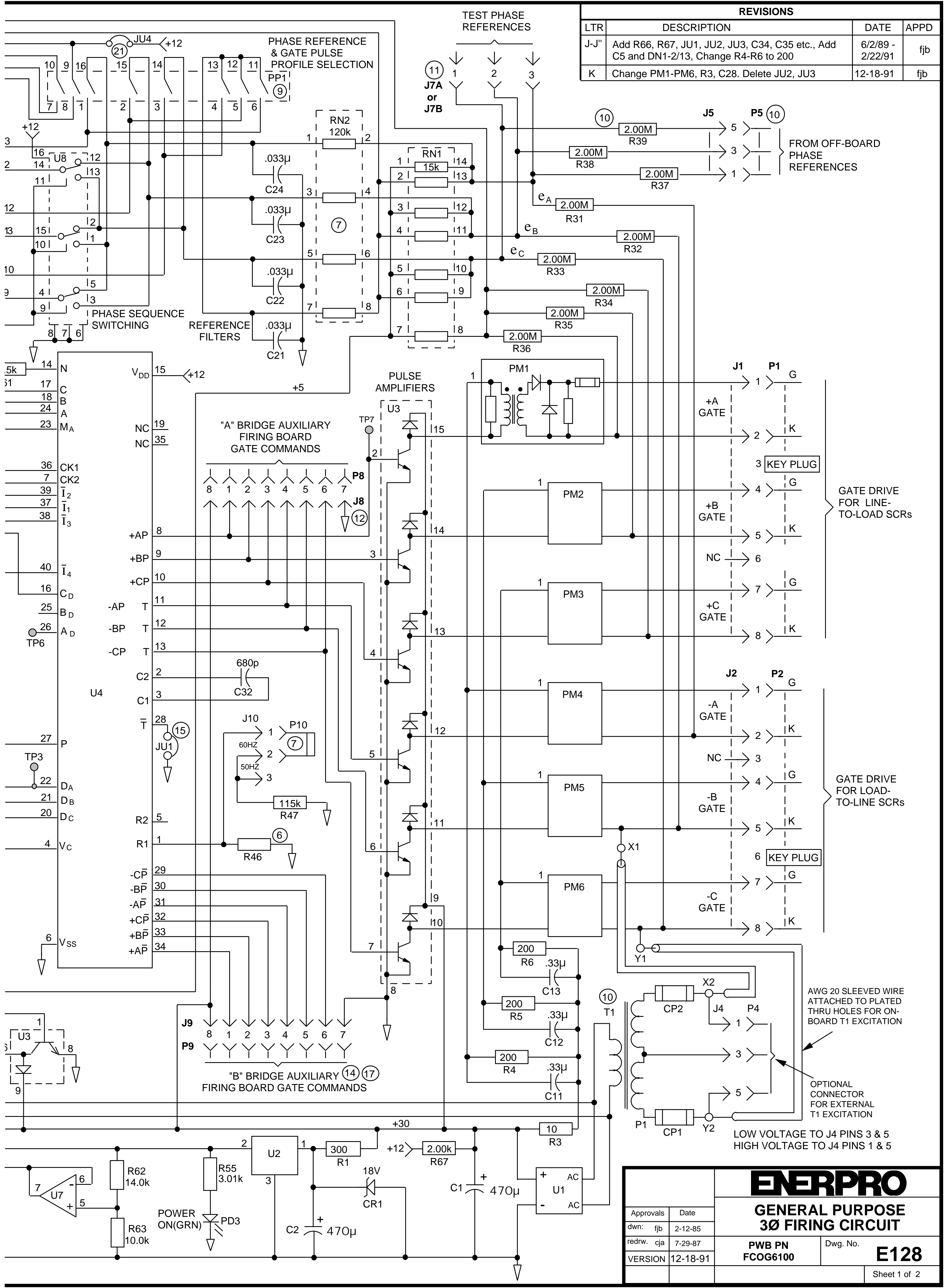
POSITION	STATUS	REFERENCE PHASE
1,2,3	OPEN	0°
4,5,6	CLOSED	-30°
1,2,3	CLOSED	-30°
4,5,6	OPEN	-30°

PP1 GATE PULSE PROFILE SELECTION

POSITION	STATUS	PROFILE
7	OPEN	120° BURST
8	CLOSED	
7	CLOSED	2-30° BURSTS
8	CLOSED	
7	CLOSED	2-60° SPACED PULSES
8 (21)	OPEN	
7	OPEN	NOT USED
8	OPEN	

See Sheet 2 for further notes

RESISTOR SELECTION	
R41	
R42	
R43	
R44	
R45	XFMR VOLTAGE SERIAL NOS.
R52	



REVISIONS			
LTR	DESCRIPTION	DATE	APPD
J-J"	Add R66, R67, JU1, JU2, JU3, C34, C35 etc., Add C5 and DN1-2/13, Change R4-R6 to 200	6/2/89 - 2/22/91	fjb
K	Change PM1-PM6, R3, C28. Delete JU2, JU3	12-18-91	fjb

GATE DRIVE FOR LINE-TO-LOAD SCRs

GATE DRIVE FOR LOAD-TO-LINE SCRs

AWG 20 SLEEVED WIRE ATTACHED TO PLATED THRU HOLES FOR ON-BOARD T1 EXCITATION

OPTIONAL CONNECTOR FOR EXTERNAL T1 EXCITATION

LOW VOLTAGE TO J4 PINS 3 & 5
HIGH VOLTAGE TO J4 PINS 1 & 5

ENERPRO													
GENERAL PURPOSE 3Ø FIRING CIRCUIT													
<table border="1"> <tr> <th>Approvals</th> <th>Date</th> </tr> <tr> <td>dwn: fjb</td> <td>2-12-85</td> </tr> <tr> <td>redw: cja</td> <td>7-29-87</td> </tr> <tr> <td>VERSION</td> <td>12-18-91</td> </tr> </table>	Approvals	Date	dwn: fjb	2-12-85	redw: cja	7-29-87	VERSION	12-18-91	<table border="1"> <tr> <td>PWB PN FCOG6100</td> <td>Dwg. No. E128</td> </tr> <tr> <td colspan="2" style="text-align: right;">Sheet 1 of 2</td> </tr> </table>	PWB PN FCOG6100	Dwg. No. E128	Sheet 1 of 2	
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