

Three-Phase High Voltage Thyristor Firing Board

Industry-Standard Digital
LSI-Based Design



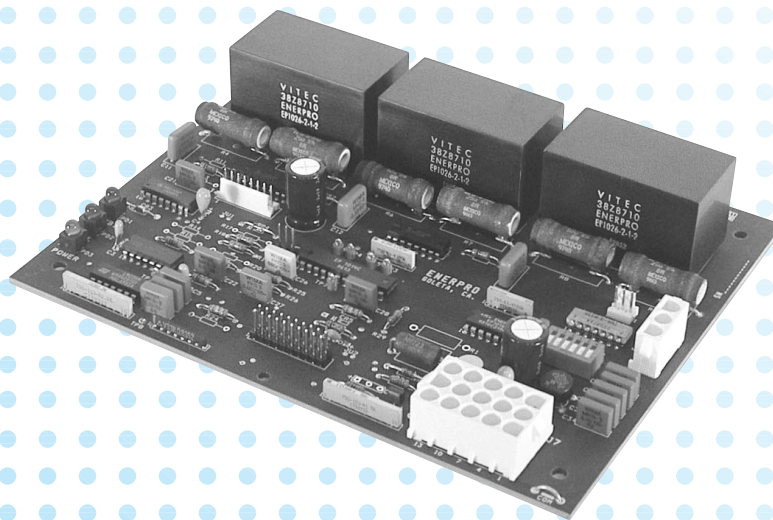
Reliable Triggering of
Thyristors with Mains
up to 2000 Vac



Increased Gate Drive



High Isolation Voltage



The Model FCOG61HV three-phase thyristor firing board utilizes the gate delay determinant of the industry standard Enerpro FCOG6100 firing board with the higher output pulse transformers and increased creepage distances for reliable triggering of large diameter (>50mm) thyristors with mains voltage of up to 2000 Vac.

Similar to the FCOG6100, the FCOG61HV employs a custom, digital LSI device for reduced component count and improved reliability. In addition, some of the key features of the FCOG61HV are:

- Insensitive to phase sequence and mains voltage distortion
- High gate isolation
- Soft and instant start/stop functions
- Phase loss inhibit
- 50/60 Hz operation

The principal departures from the FCOG6100 design are:

- Pulse transformers with larger ferrite cores and 3-flange bobbins for increased gate drive and higher isolation voltage
- Two pulse transformers per module for better board space utilization
- Line and load sensing resistors inside the pulse transformer modules to eliminate exposed high potential conductors
- No on-board transformer
- Reversing converter/controller capability deleted

A low leakage inductance 1:1 ratio pulse transformer is available for converter applications where a rapid rate-of-rise of gate current and substantial open circuit voltage is necessary for proper thyristor triggering in high di/dt applications. And, a higher inductance 2.5:1 step down pulse transformer is specified for gating inductively loaded converters or controllers where higher amplitude sustaining gate current pulses is required.

3-PHASE FIRING BOARD

THEORY OF OPERATION

The thyristor gate delay control circuitry is based on the biased detector phase locked loop (PLL) principle that is the basis of Enerpro's industry-standard 2-pulse, 6-pulse and 12-pulse thyristor firing boards.

Phase Reference

The phase reference signal for each mains voltage is collected by a high value resistor (possible values are 1.5 m Ω , 2.0 m Ω , 3.0 m Ω and 4.0 m Ω) installed in each pulse module and connected to the cathodes of the load-to-line thyristors. A second high value resistor is provided in each pulse module to sense the load voltage. The first high resistance resistors together with three 15 k Ω resistors and three low pass filters, attenuate the ac mains voltages to a level suitable for input to the phase reference differential comparators. The low pass filters remove most of the distortion from the reference voltages — distortion caused by non-sinusoidal converter input current acting on the supply impedance. The low pass filter's 60° phase shift is effectively cancelled by selecting an inverted reference voltage from another phase as a comparator input. A phase sequence sensing circuit modifies the reference voltage selection depending on the phase sequence.

For converter gating, a programming plug is configured to apply line-to-line filtered reference voltages to the comparator inputs. The 50% duty cycle comparator output logic signal thus lags the zero crossing of the mains phase voltage by 30° as required for converter gating.

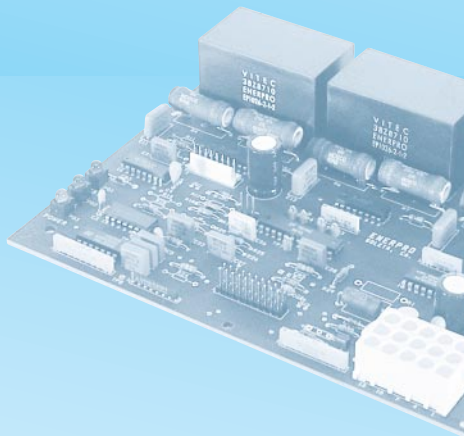
The comparator output signals must track the mains phase voltage when the firing circuit gates an ac controller. This is accomplished by configuring the programming plug to apply a low level analog of the mains neutral voltage to the non-inverting comparator input. The neutral voltage signal is derived with an additional R-C circuit that sums and filters the three attenuated reference signals. Use of this fictitious neutral signal allows the firing circuit to function properly when the mains voltage has a substantial voltage unbalance from line to ground.

The three phase reference comparators and the three analog switches that select the proper comparator input reference signal as a function of the phase sequence are contained in a 16-pin CMOS LSI device. This device also provides a +5V reference voltage for the firing board.

Gate Delay Determinator

A 24-pin CMOS LSI device contains the voltage controlled oscillator (VCO) and the logic circuitry of the delay determinator PLL. Inputs to the device include the three-phase reference signals described above and the VCO control voltage. This control voltage is the output of an op amp that sums the three EX-OR phase detector outputs of the LSI device with a signal proportional to the gate delay command voltage.

When the PLL is in lock, the average VCO control voltage is constant and proportional to the mains frequency. This dictates that the sum of the three phase detector outputs and the delay angle command be a constant voltage which in turn implies that a change in the delay angle command be accompa-



nied by an equal change in the voltage output of the phase detectors. Since the input to the phase detectors is the difference between the phase of the mains voltage and the phase of the delayed gate command signal, the gate delay angle (which is the difference between these two angles) is also proportional to the delay angle command voltage.

The delay determinator VCO creates a clock frequency of 384 times the mains frequency (384xF). This high frequency clock is first divided by 64 to produce a lower frequency clock at six times the mains frequency (6xF). The 6xF clock is then divided by six and split into three delayed (by a degrees), 120° spaced 1xF phase reference signals.

Two gate pulse profiles are available to suit the application.

The two-burst pulse profile economizes on gate power and is used when gating converters and controllers that feed a relatively low inductance load. It is obtained by ANDing the three delayed 1xF reference signals with the 384xF and 6xF clocks. Each gate pulse is 50% duty cycle with a pulse width of $22\mu\text{s} + 4\mu\text{s}$. The first burst begins at delay angle ∞ and the second begins at $\infty + 60^\circ$.

A single 120° wide gate pulse burst beginning at delay angle ∞ is obtained by ANDing the three delayed 1xF reference signals with the 384xF clock. This pulse profile is used for gating converters and controllers having a highly inductive load.

Gate Pulse Amplification and Isolation

The thyristor gate command signals are amplified by transistors to energize the primary windings of the six pulse transformers. An RC circuit supplied from unregulated 34 to 44 Vdc accentuates the

first pulse in the gate current burst relative to the succeeding pulses. Each pair of gate pulse transformers is housed in a potted module along with associated primary and secondary noise suppression resistors, secondary output coupling diode, output fuse and line and load voltage sensing resistors.

One of two gate pulse transformer designs may be selected to suit the application.

The EP1025 pulse module serves for gating converters or resistively loaded ac controllers where the thyristor anode current is characterized by high di/dt during commutation. The pulse transformers of the EP1025 have a 1:1 ratio for high open circuit voltage. A relatively small number of turns gives low leakage inductance and a high rate-of-rise of gate current. The EP1025 open circuit voltage for the first pulse in the burst is approximately 40 V for a maximum dc supply voltage of 44 Vdc. The peak short circuit current and initial rate-of-rise of the first pulse are approximately 1.3 A and 1.25 A/ μs for a 44 Vdc supply. The corresponding sustaining pulses are characterized by 17 V open circuit and 0.5 A short circuit. The sustaining pulses decay sharply to approximately 0.20 A at the end of the pulse.

The EP1026 pulse module is used for gating ac controllers where the load power factor angle may exceed the thyristor gate delay angle. Under this condition, the thyristor is fully conductive; the anode current being initiated by the sustaining gate pulses. The $22\mu\text{s} + 4\mu\text{s}$ gap in the gate current results in a thyristor ignition delay of up to 26 μs . The ignition delay may become substantially greater than 26 μs if the sustaining gate pulses decay to less than the rated minimum-gate-current-to-trigger (I_{GT}) of typically 0.25 A. The pulse transformers of the EP1026 module have increased primary

turns and a 2.5:1 step down ratio. This results in a peak current and rate-of-rise for the first pulse of about 1.3 A and 0.6 A/ μs with a 44 V supply. The sustaining pulses have a peak of about 1.8 A and decay to about 0.7 A at the end of the pulse. This is well above the thyristor I_{GT} , thus preventing excessive ignition delay.

The primary and secondary windings of the gate pulse transformers are wound side-by-side on a 3-flange bobbin. This construction results in a 4000 Vrms isolation rating. The primary-to-secondary circuit board creepage distance is 15.7 mm (0.62").

Phase Loss Sensing

The phase loss (PL) circuit operates from an input signal formed by summing and filtering the three 120° spaced square wave outputs of the reference comparators. In normal operation, the filtered square waves sum to a dc level with a superimposed 3xF (180 Hz for 60 Hz mains) triangle wave. When one phase voltage is abnormally low, the comparator outputs deviate from the correct 120° phase shift and 50% duty cycle. As a result, the filtered composite comparator signal shows a shift in dc level along with 1xF and 2xF Hz frequency components. These changes are detected by a window comparator. When the PL input signal peaks exceed the upper comparator threshold or fall below the lower comparator threshold, the comparator output goes low to signal a PL fault and reset the soft-start circuit. The soft-start circuit activates the PLL delay determinator to ramp the gate delay out to its maximum angle before inhibiting the thyristor gating.

Gating remains inhibited until the phase loss condition is cleared. At that time, the PL comparator output goes high, allowing the gate delay angle to ramp down to its normal value and bring the rectifier dc output back up to its pre-fault level. The

response time of the phase loss detector is approximately five ms (6 ms at 50 Hz).

A PL fault is reported to the board I/O connector via an open collector transistor. The transistor sinks current from a customer-supplied pullup resistor when a PL fault is present.

Load Voltage Sensing

Load voltage sensing is often useful when gating ac controllers. This is accomplished by a second high value resistor (the first high value resistor senses the mains voltage) in each pulse module which connects to the controller load terminals via the cathode connections to the line-to-load thyristors. The low voltage terminal of the three load connected resistors are connected together to a 15kΩ resistor which in turn is connected to the +5 V bias voltage. The resultant signal load voltage signal is designated as E_L in the schematic diagram. The waveform of the load voltage signal is a composite analog of the successive thyristor blocking voltages, biased at 5 V and alternating in polarity to produce a 3xF fundamental frequency.

Soft-Enable/Inhibit

The soft-enable circuit responds to an externally applied NOT (I2) signal (active low inhibits) as well as to the PL fault signal as described above. The soft-enable time is set by the product of resistor R11 and capacitor C4. The standard time constant is $100\text{ k}\Omega \times 22\text{ }\mu\text{F} = 2.2\text{ s}$. This time constant causes the gate delay angle to ramp from maximum to minimum in approximately 2.2 ms. Soft-enable times in the range of 50 ms to 3.0 s can be specified.

The soft-inhibit circuit ramps the gate delay from minimum to maximum and then inhibits the thyristor gate outputs. The soft-inhibit time constant is the product

of R13 and C4. The standard soft-inhibit time constant is $10\text{ k}\Omega \times 22\text{ }\mu\text{F} = 220\text{ ms}$. The resulting time for the delay angle to ramp from minimum to maximum is approximately 220 ms. Soft-inhibit times in the range of 200 ms to 2.00 s can be specified.

Instant Enable/Inhibit

The instant enable/inhibit circuit responds to an externally applied NOT (I1) signal (active high enables) to instantly enable or inhibit the thyristor gating.

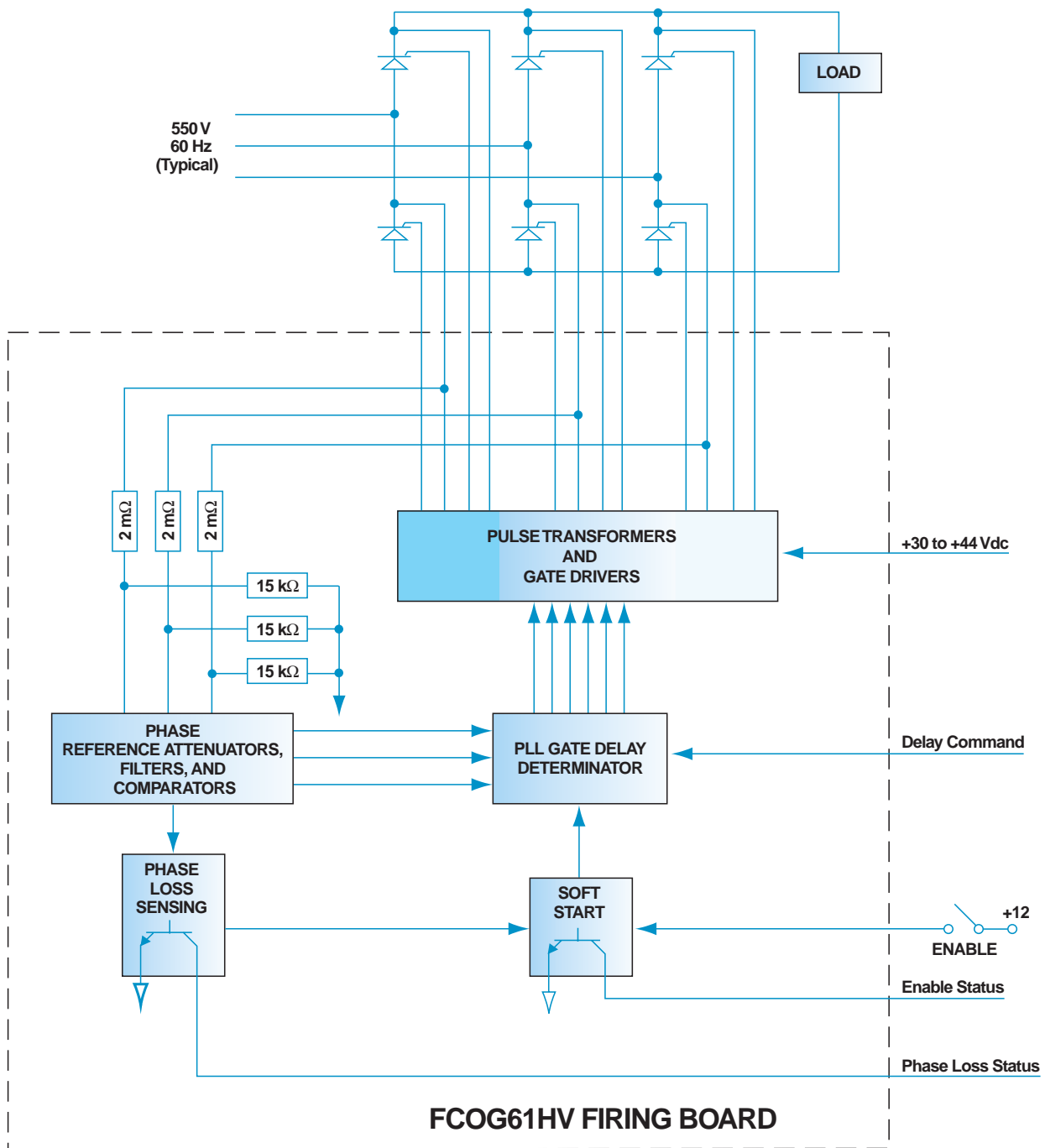
The status of the soft and instant enable/inhibit circuits is reported to the I/O connector by an open collector transistor. A customer-supplied pullup resistor creates a logic status signal when gating is enabled.

50 Hz Operation

The following circuit modifications are required for operation with 50 Hz power:

1. The VCO timing resistance is increased by 6/5 by changing the position of a shorting plug.
2. The phase reference filter resistor network is changed from 150 kΩ to 180 kΩ.

MAXIMUM RATINGS	
Board Supply Voltage (Vac)	24 to 34
Maximum AC Demand (VA)	25
Board Supply Voltage (Vdc)	30 to 44
Maximum DC Demand (W)	10
AC Mains Voltage (Vac)	
In Rain, Dust and Snow Environment	600
In Water Droplet Environment	1000
In Low Humidity Environment	2000
Pulse Transformer	
Hipot (Vac) / 60s	4000
Operating Temperature (°C)	-5 to +85
Storage Temperature (°C)	-65 to +85
ELECTRICAL CHARACTERISTICS	
Sensing Resistances (MΩ)	1.5, 2.00, 3.00, 4.00 (user-specified)
Delay Command Range (Vdc)	0 to 5.0 or 0.85 to 5.85
Delay Angle Range (°C)	(user-specified)
Delay Angle Tracking (°C)	120 ± 1.0
Soft-Stop Time (ms)	700 (standard)
Soft-Start Time (ms)	50 to 3000
Pulse Profile	Two 30° bursts of 32 pulses One 120° burst of 128 pulses
Pulse Width	
50 Hz (ms)	24 to 29
60 Hz (ms)	20 to 24
Pulse Modules (Model EP1025)	
First Gate Pulse:	
Short Circuit Current (A)	1.3
Short Circuit Rate-of-Rise (A/μs)	0.9
Open Circuit Voltage (V)	40
Follow-on Gate Pulses	
Short Circuit Current (A)	0.6
Pulse Modules (Model EP1026)	
First Gate Pulse:	
Short Circuit Current (A)	1.8
Short Circuit Rate-of-Rise (A/μs)	0.9
Open Circuit Voltage (V)	15
Follow-on Gate Pulses	
Short Circuit Current (A)	1.0
MECHANICAL SPECIFICATIONS	
Printed Circuit Board	
Dimensions	191 mm x 152 mm



ORDERING GUIDE



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MODEL **3-Phase High Voltage Thyristor Firing Board**

CODE	THYRISTOR ARRANGEMENT
0	
1	6 SCRs

CODE	INDUCTIVE LOAD
0	No
1	Yes

CODE	AUXILIARY FIRING BOARD?
0	No
1	Yes

CODE	REGULATOR BOARD?
0	No
1	Yes

CODE	MAINS VOLTAGE
XX	Voltage + 10

CODE	MAINS FREQUENCY
XX	Frequency + 10

CODE	MINIMUM DELAY ANGLE
XX	

CODE	MAXIMUM DELAY ANGLE
XXX	

CODE	DELAY COMMAND VOLTAGE
0	0 to 5 V Command
1	0.85 to 5.85 V Command
2	4 to 20 mA Command

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Enerpro Applications Engineers are available by telephone, fax or email to answer any questions about your thyristor control board applications.