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**OPERATING MANUAL
FOR A MODEL FCRO4100
SINGLE PHASE FIRING CIRCUIT BOARD**

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INTRODUCTION

This manual is intended to familiarize the user with the salient features and specifications of the model FCRO4100 single phase firing board. A simple installation procedure is included together with typical firing circuit signal waveforms and connection diagrams.

REFERENCES

1. Schematic Diagram, E168, "Single Phase 4-SCR Bipolar Firing Circuit/Regulator", Model FCRO4100.
2. Schematic Diagram, E216, "Single Phase Transition Inhibit and Voltage Regulator", Model PTIR-1.
3. Schematic Diagram, E417, "Single Phase Voltage Regulator and Current Limiter", Model VRCL1P-1.
4. Operational Description, "VRCL1P-1 Regulator"
5. Product Guide, PD736, "Auxiliary SCR Firing Circuits".
6. Product Guide, "Three Phase Regulator Packages".
7. Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Oct. 17-19, Long Beach, California.

PRODUCT DESCRIPTION

APPLICATION

The general purpose single phase firing circuit board produces four sets of high current SCR gate pulses. Each set consists of a burst of 50% duty cycle pulses having a carrier frequency that is a phase locked multiple (256) of the mains frequency. The initial pulse of each burst is delayed by an angle from the zero crossing of the associated mains voltage. The delay angle varies in negative proportion to a voltage or milliamp delay enable command signal. Each gate pulse burst has a duration of 180° - . This provides an adaptable circuit suitable for use in a wide range of SCR controllers or converters (rectifiers). The range of applications is further enhanced by the use of regulator boards and/or auxiliary firing boards. These boards extend the FCRO4100's functionality to include:

- paralleled SCR circuits
- four-quadrant converters
- remote operation of SCR's

BOARD MOUNTED CONNECTORS

The firing board utilizes AMP Mate-N-Lok™ connectors to simplify maintenance and trouble shooting.

Gate/Cathode Connectors (J1 and J2)

The SCR gate/cathode interface is provided by a 6-position header, J1, and a 5-position header, J2, Mate-N-Lok™ right angle headers² and mating plugs, P1 and P2. Plug P1 accesses the gates and cathodes of the SCRs used in a single in-line ac controller or two SCR converter configurations. Similarly, plug P2 accesses the gates and cathodes of the two additional SCRs used in four SCR configurations.

Power Supply Connector (J3)

¹ This product guide discusses a variety of regulators used in conjunction with our 3Ø firing boards. However, the following models can also be used with the FCRO4100 1Ø firing board: CR400, CTRCT-1, CTRCT-2, CVCI-1, ISOVLCL-1, and ISOVLCL-2.

² Vertical headers are available upon request.

In addition to providing control power, this signal is used as the phase reference by the phase-locked-loop. Therefore, it is imperative that the ac voltage supplied as control power be in-phase with the ac voltage supplied to the SCR's.

The board mounted 24VA power supply transformer is typically supplied with a dual voltage primary. This primary is normally energized by connection with insulated wire from the mains voltages to positions 1 and 5 or 3 and 5 of 5-position Mate-N-Lok™ right angle header J3. Positions 1 and 5 of J3 are used with the higher voltage while pins 3 and 5 are used with the lower voltage.

Control Signal Connector (J4)

The firing board is connected to the gate delay command and inhibit controls through a 12-position Mate-N-Lok™ connector J4. This connector also accesses the outputs of the 24Vac board mounted transformer, the 30Vdc rectifier and the regulated +12Vdc and +5Vdc outputs. With the board mounted transformer installed, approximately 10 watts of ac or dc power is available from J4 to power lamps or a control relay. These connections are outlined in greater detail in Table 1.

Positions of J4	Connections	Supporting information
1 & 2	24Vac	The board AC power from the secondary of T1
3	+30Vdc	Rectified 24 Vac (available for customer use)
4	Instant Inhibit	Instantly inhibit or enable SCR gating by applying or removing +12Vdc.
5	Polarity transition	4-quadrant applications
6	+12Vdc	Board power (available for customer use)
7	+5Vdc	Board power (available for customer use)
8	Common	Circuit common
9	Enable indication signal	Install R5 for desired lamp or relay coil voltage
10	Signal High	0 to +5.0 delay angle command signal
11	Common	Circuit common
12	Soft Inhibit	Soft start or stop SCR gating by opening from or connecting to ground (pin 8 or 11)

Table 1. J4 Control Signal Connector - Pin Designations

Feedback Signals Connector (J5)

Current and voltage feedback signals are supplied to a 4-position Mate-N-Lok™ header, J5, through mating plug P5. Positions 1 and 2 of J5 are designated for current feedback connections. If an ac current signal is used, a rectifier U5 and a burden resistor R4 must be installed. R4 is then selected as required to obtain a 1.0Vdc full load feedback signal. For use with a dc feedback signal, omit U5 and jumper pads 1-4 and 2-3 of U5.

Position 3 of J5 is designated for a current limit command signal. Position 4 is designated for voltage feedback signal. An optional regulator board PTIR-1 or VRCL1P-1 regulator board must be installed for use with these signals. Refer to references 2, 3, and 4 for details on these regulator boards .

Auxiliary Regulator Board Connector (J6)

Key firing board signals are brought out to a 14-position vertical circuit board header, J6. This allows either the VRCL1P-1 or PTIR-1 regulator board to be conveniently mounted on stand-offs above the firing board.

Auxiliary Firing Board Connector (J7)

One 6-position cable header, J7, is provided to connect one set of 4 gate command logic signals, as well as +30Vdc power and circuit common, to the FCOAUX60 Auxiliary Firing Board. This allows for gating an additional set of four SCRs as required by the circuit configuration.

Frequency Selection Connector (J8)

A 3-position header, J8, is used to select between 50Hz and 60Hz operation. In 60Hz operation R13 is connected in parallel with R12. In 50Hz operation J8 removes R13 from the circuit in order to maintain TP7 at 5.0Vdc.

GATE DELAY COMMAND

The gate delay command signal, SIG HI, may be a zero to 5.0Vdc voltage signal or a current signal with an upper limit of 50mA. The input resistance presented to the delay command signal is determined by the parallel combination of R11 and 9.99k (R19 and R7) which is connected in shunt with the control signal input. When the gate delay command is a current signal, R11 is selected to provide a 5.0Vdc level at the maximum command signal current. For typical 4-20mAdc current signal input, R11 is select as 249 .

BIAS AND SPAN ADJUSTMENT

Two 5K potentiometers, R6 and R7, provide delay angle bias and span adjustment capability. These potentiometers will adjust the FCRO4100 boards minimum and maximum delay angles as related to the applied SIG HI command signal.

Increase the command signal input to the desired minimum input level or until the low signal inhibit (described below) clears, whichever is higher. Then adjust the BIAS potentiometer, R6, to obtain the desired minimum SCR output. Now increase the command signal to the maximum input level and adjust the SPAN potentiometer, R7, as required to obtain the desired maximum SCR output. Repeat these steps until the optimum response is obtained.

BIPOLAR FIRING OPTIONS

Two-quadrant four-pulse gating is provided by the FCRO4100 Firing Board. The FCOAUX60 Auxiliary Firing Board extends the application to four-quadrant four-pulse converters. An optional polarity transition timed gate inhibit board, model PTIR-1, is available for four-quadrant converters. The PTIR-1 will inhibit SCR gating for approximately 100ms upon a transition of the polarity command signal, P.

A logic one P signal at J4 position 5 (the normal state due to pull-up resistor RN4-7/8) enables the gate drive from the main firing board and inhibits the gating from the auxiliary firing board. A logic zero P signal, provided by an active low, inhibits the main board and enables the auxiliary board.

Four-Quadrant 2-Pulse Converter

Four-quadrant two-pulse gating from the FCRO4100 firing board is achieved by jumpering JU2 on the board. The gate drive to the positively poled SCRs is then provided by pulse modules PM1-PM2, and to the negatively poled SCRs by PM3-PM4.

Four-Quadrant 4-Pulse Converter

Four-quadrant four-pulse gating is obtained from the main firing board and auxiliary firing board by connecting the six-conductor inter-board cable to J7 on the main firing board. Positively poled SCRs are then gated by the main firing board, negatively poled SCRs by the auxiliary firing board.

ENABLE/INHIBIT DISPLAY SIGNAL "L"

An open collector transistor is provided for use as an external Enable/Inhibit indicator. This signal can be accessed at J4 pin 9 and can sink up to 500mA. A current limiting resistor, R5, can be selected to provide the proper voltage drop. Typically, this signal is used in conjunction with an external 24Vdc relay, the FCRO4100 unregulated +30Vdc supply, and limiting resistor R5 = 200 .

GATE INHIBITS AND INHIBIT INDICATOR LED PD1

SCR gating is inhibited by making either or both of the inhibit signal points, designated as NOT(I₁) and NOT(I₂) and appearing at pins 4 and 12 of J4, a logic zero or by detecting a low signal input.

Instantaneous Inhibit/Enable

In the case of the instantaneous inhibit, NOT(I₁), resistor RN4-3/4 on the firing board is provided to pull the NOT(I₁) signal low if the connection between NOT(I₁) and +12 Vdc is opened. This ensures that SCR gating is inhibited if plug P4 is inadvertently disconnected. In applications where the instantaneous gate inhibit function is not utilized, a jumper wire is installed between pins 4 and 6 of P4 to hold NOT(I₁) at +12 Vdc when P4 is installed in J4.

Soft Inhibit (Soft-Stop)

The inhibit signal NOT(I₂) is connected to +12 Vdc through pull-up resistor RN4-5/6 on the firing board. When NOT(I₂) is grounded, the gate delay angle is ramped to the maximum delay angle before gating is inhibited. The soft-stop feature is activated by externally connecting J4-12 to either J4-8 or J4-11. This allows C2 to discharge through CR2 and R15. The soft-stop time is approximately:

$$t_{\text{soft-stop}} = 1.84(R15)(C2)$$

where R is in k , C is in μF, and t is in msec

As C2 exponentially discharges, the output of the voltage follower U1B tracks the decreasing voltage on C2. Diode CR5 then becomes conductive, reducing the voltage at the non-inverting input of the PLL summing amplifier, U1D. The output of this amplifier thus injects a decreasing current into the PLL summing/filter network which causes a compensating increase in the EX-OR phase detector in the PLL LSI device as required to maintain a constant dc level at the VCO control voltage input pin, U3-22, of the LSI device. The increase in the EX-OR gate output is accompanied by an increase in the gate delay angle and a decrease in the fraction of the mains voltage applied to the load.

When the exponentially decreasing voltage follower output U1B drops below the approximately 1.1V threshold of the inhibit inverter U1C, the output of the inverter goes low. This logic zero state is applied to the inhibit terminal of the PLL LSI device U3 to inhibit the SCR gating.

Soft Enable (Soft-Start)

Breaking the connection between J4-12 and either J4-8 or J4-11 activates the soft-start feature. This allows C2 to charge through R14 and RN4-5/6 to give a soft-start time of approximately:

$$t_{\text{soft-start}} = 0.58(1.5 + R14)(C2)$$

The output of the voltage follower U1B tracks the exponential rise of the voltage on C2. As described above, the voltage follower output enables the SCR gating when it ramps up to 1.1V. The follower output continues to increase as C2 charges, causing diode CR5 to couple an increasing voltage to the non-inverting input of the PLL summing amplifier U1D. In response the gate delay angle decreases and the SCR conduction increases to apply an increasing fraction of the mains voltage to the load.

When the voltage follower output rises to about 4.5V, CR5 ceases to conduct and the voltage at the non-inverting input of U1D becomes 5.0V. The output of U1D then responds only to

the output of the error amplifier U2A. If the firing circuit is configured for open loop operation, steady state gate delay angle varies in negative proportion to the delay angle command, SIG HI. In the closed-loop mode, the gate delay angle responds to the difference between the current (or voltage) command and the current (or voltage) feedback signal.

Low Signal Inhibit

The output of the Low Signal Inhibit comparator, U2D, is at the logic 1 state when the SIG HI gate delay command is less than the 0.478V comparator threshold voltage. This logic 1 state is applied to the summing junction of the inhibit signal inverter, U1C, to form a logic 0 at the inhibit terminal of the PLL LSI device U3. The result is that SCR gating is inhibited when SIG HI is less than 0.478V. Omit diode CR6 to eliminate the Low Signal Inhibit feature.

Inhibit Indicator: LED PD1

The anode of the red LED indicator PD1 is pulled up to +12V by resistor R21. The cathode of PD1 is connected to the open collector output of transistor network device U4B so that photo diode current flows when the transistor collector is in the active low state. The input of U4B is pulled up to +30V by resistor R5 or up to +12V by resistor RN7-3/4 if R5 is not installed. The input of U4B is pulled down by the collector of U4A when tin input of U4A is driven low by a logic 0 state $\{\text{NOT}(I_2) = 0\}$ at the output of the inhibit comparator U1C. The net result is that the Inhibit Indicator LED is illuminated when the SCR gating is inhibited.

Power-On Reset

The power-on reset circuit consists of resistors R1 and RN6-7/8, zener diode CR1, and transistors Q1 and Q2. These components reset the soft-start circuit in response to an under-voltage condition at the output of the power supply rectifier U6.. Figure 1 shows the relevant components.

At the instant that ac power is applied to the rectifier U6, the voltage at the cathode of CR1 is less than the 15V zener voltage. Therefore, CR1 is not conductive and no current flows into the base of transistor Q1. With Q1 in the cutoff state, all current in its collector load resistor RN5-1/2 flows into the base of transistor Q2. The collector of Q2 thus goes to the active low state and clamps the voltage on the soft-start capacitor C2 to about 0.3V. The output of the voltage follower U1B is also about 0.3V and this signal voltage is applied to the non-inverting input of the inhibit inverter U1C. The signal voltage is less than the nominal 1.1V threshold voltage at the inverting input of U1C. Thus at power-up, the inverter output, and the inhibit pin of LSI device U3 to which it is connected, are at a logic zero state and SCR gating is inhibited.

About 50msec after ac power is applied to U6, the rectifier filter capacitor C1 is close to fully charged and the unregulated supply voltage has risen to about 30V. Zener diode CR1 conducts to apply current, limited by 220 resistor R1, to the base of Q1 (CR1 also reduces the dissipation of the +12V regulator U7 by limiting its input voltage to about 15.5V). Q1 conducts and effectively grounds the base of Q2. Q2 becomes an open circuit, allowing the voltage at the non-inverting input of the soft-start voltage follower U1B to increase to about 5.5V (the forward drop of diode CR4 plus 5V). Diode CR5 at the output of the voltage follower then becomes non-conductive, thus effectively disconnecting the soft-start circuit from the PLL summing amplifier, U1D.

Note: In certain systems the power-on reset circuit will be intermittently activated due to poor ac line quality. In this case the system will appear to oscillate at an output level less than maximum. If the voltage across CR2 is oscillating, the power-on reset circuit is active. The circuit can be defeated by removing Q2 (consult an Enerpro applications representative prior to removing Q2) or its sensitivity reduced by changing CR1 and/or R1 (this is the preferred method of operation).

DELAY ANGLE FREQUENCY RESPONSE

Dynamic frequency response specifications are: -3dB attenuation at 67Hz, and 45° phase shift at 57Hz.

The simplified delay angle frequency response is:

$$\frac{\text{SIG HI}}{\text{VOLT}} = \frac{34}{j/358 + 1} \left(\frac{\text{deg}}{\text{Volt}} \right)$$

GATE PULSE PROFILE

The firing circuit uses a phase-locked-loop (PLL) circuit locked to the single phase mains voltage. The PLL oscillator output is counted down and decoded into four 0° to 180° wide delayed logic signals. The 0° to 180° wide delayed logic signals are modulated by the 15,360 Hz (256 * 60) PLL Voltage Controlled Oscillator (VCO) output signal. The modulated signals output to the darlington transistor array, U4. The collectors of U4 are connected to +30Vdc through the pulse module primaries and pulse shaping components R2, R3, C5, and C6.

Figures 3 and 4 show the pulse transformer output waveform into a 1.0 non-inductive resistor load.

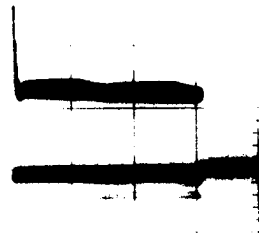


Figure 3. 120° burst of pulse output (.5 A/div)

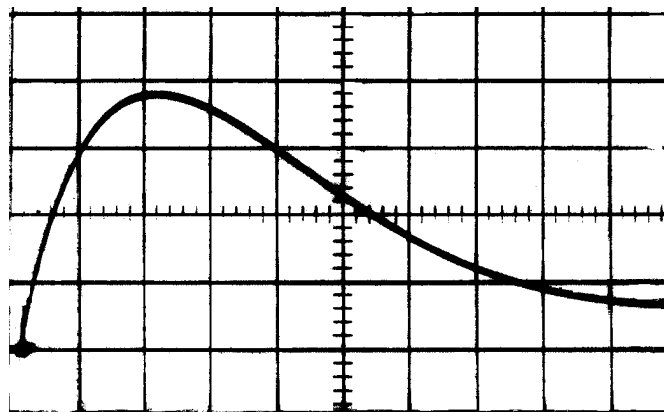


Figure 4. Initial pulse detail (.5 A/div, 2 μs/div)

GATE PULSE AMPLIFIER

Circuitry shown in drawing E168 consisting of transistor array U4, resistors R2 and R3, capacitors C5 and C6, and gate pulse isolation modules PM1 through PM4 amplify and shape the thyristor gate current pulses. Each pulse module consists of a 1.67:1 ratio pulse transformer tested for 3500Vrms isolation, two secondary diodes, noise suppression resistors across the primary and across the gate drive output, and a fuse in series with the output.

ELECTRICAL SPECIFICATIONS

The electrical specifications of the General Purpose Firing Board are summarized in the table below. Part numbers refer to drawing E168 revision I

Characteristic	Performance Requirement	Supporting Information
1. Board mounted power supply for control electronics and SCR gate drive.	Connect to mains at J3-5 and J3-1 for 240/480V or J3-3 and J3-5 for 120/240V.	24VA 1Ø 50/60Hz fused board mounted transformer T1. Center-tapped primary connected for 240V or 480V.
2. SCR gate waveform.	Pulse Profile: 180 - burst with a 32.6µs pulse width.	
3. Input control signal.	0 Vdc to 5.0 Vdc control signal. Input impedance is 10.0k .	Option : a shunt resistance (R11) across signal input can be selected for milliamp control signal. R11 = 249 for 4 to 20mAdc current control signal.
4. Gate delay steady-state transfer function.	Increase in command voltage produces a proportional decrease in gate delay angle, .	max. and min. change equally with change in R _{bias} (R6). (max- min) changes with R _{span} (R7).
5. Gate delay dynamic transfer function bandwidth.	Attenuation = -3dB at 67Hz. Phase shift = -45° @ 57Hz.	Frequency response can be modified by changing summing amplifier parameters.
6. Effect of frequency.	/ f = 1.5°/Hz. For 50Hz operation, compensate by removing R13.	Jumper J8 for 50/60 selectable operation
7. Lock acquisition time.	Approximately 30ms.	Gating is inhibited for 20ms or longer at power-on. Inhibit period depends on Soft-Start time constant.
8. Soft-Start	Gating commences at max. and exponentially decays to the commanded delay when NOT(I2) is ungrounded (J4-12).	Soft-Start time constant is set by C2 and R14. $T = (1.5k + R14)(C2)(0.579)$ T in ms, R in k , C in µF R14 20.0k
9. Soft-Stop	Gate-delay angle ramps to max. before being inhibited when NOT(I2) is grounded.	Soft-Stop time constant is set by C2 and R15. $T = R15(C2)(1.84)$ R15 1.0k
10. Power-on inhibit.	Inhibit circuit is activated at power-on.	Same delay angle response as with the soft-start circuit.
11. Low Signal Inhibit	Inhibit circuit is activated if SIG HI < 0.5Vdc.	Eliminate this feature by removing CR6.
12. Instantaneous inhibit.	Opening the connection of NOT(I1) (P4-4) to +12V instantly inhibits SCR gating. Closing the connection of NOT(I1) to +12V instantly enables SCR gating.	Gating is inhibited if P4 is removed.
13. Peak gate drive open circuit voltage	15V	With a 30Vdc supply voltage

14. Peak gate drive short circuit current.	1.7A	Measured with a 30 Vdc supply voltage and a 1.0 load resistor
15. Gate drive current rise time(short circuit)	.5A in .5μs	Measured with a 30 Vdc supply voltage and a 1.0 load resistor
16. Frequency sensitivity	2.6°el./Hz	
17. Temp. sensitivity	±2°el. for 0° C<Ta<70° C	
18. Ambient temperature.	0°C to 70°C	

TYPICAL CONNECTION DIAGRAMS

Figures 5 through 10 show the basic connections required for several common uses of the FCRO4100 firing board. If additional information is required, please contact the Enerpro applications department.

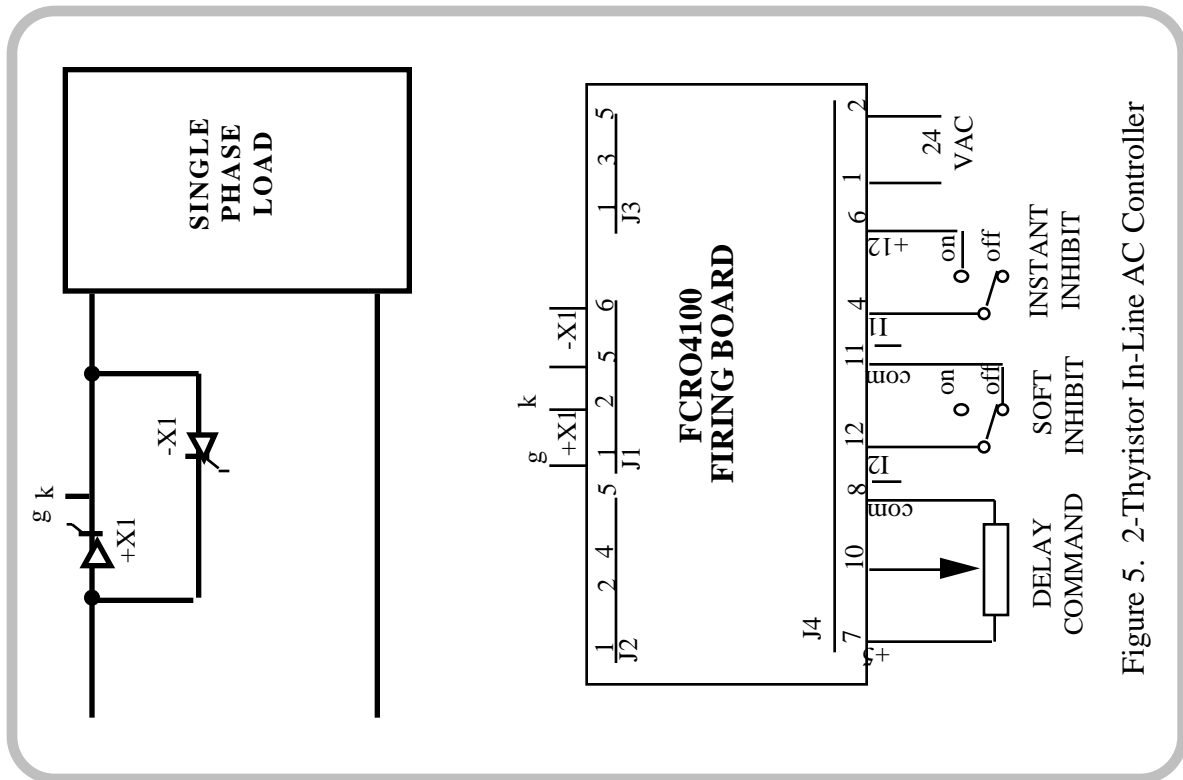


Figure 5. 2-Thyristor In-Line AC Controller

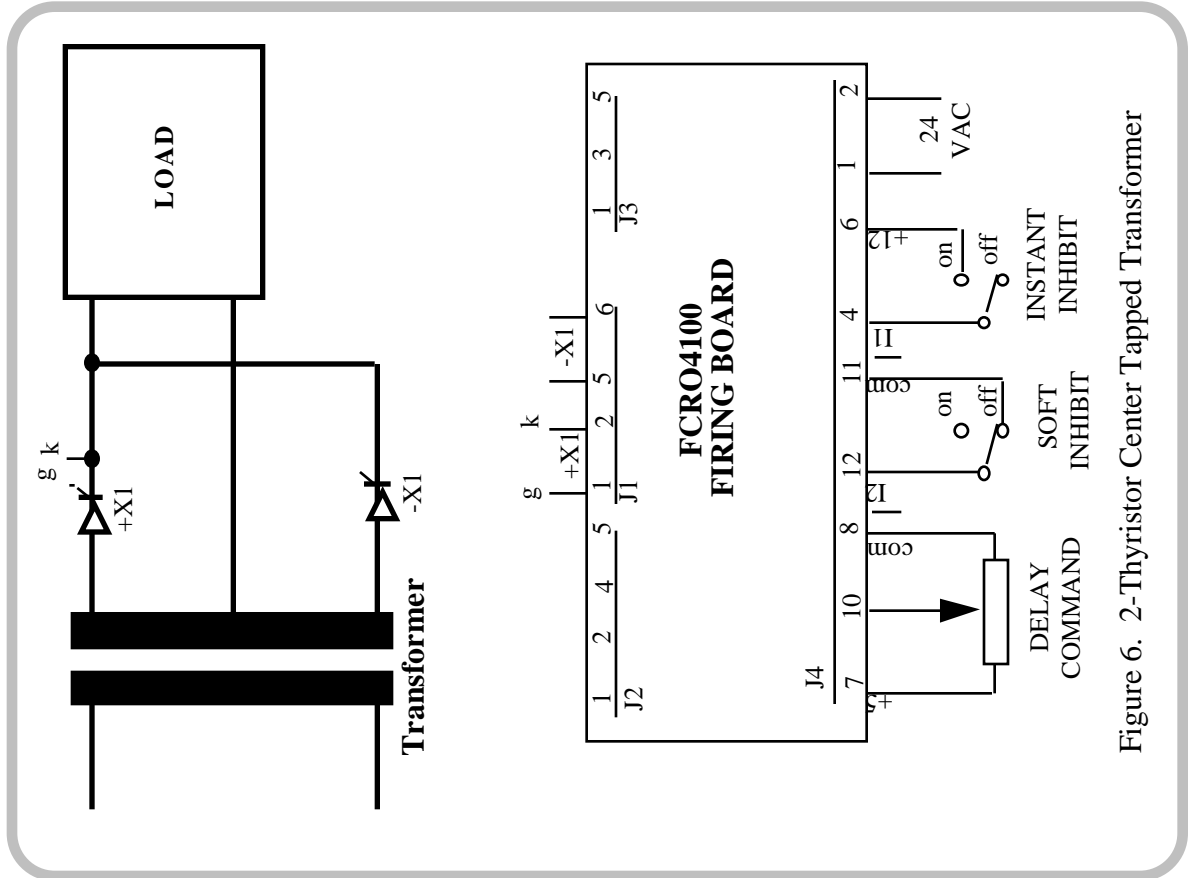


Figure 6. 2-Thyristor Center Tapped Transformer

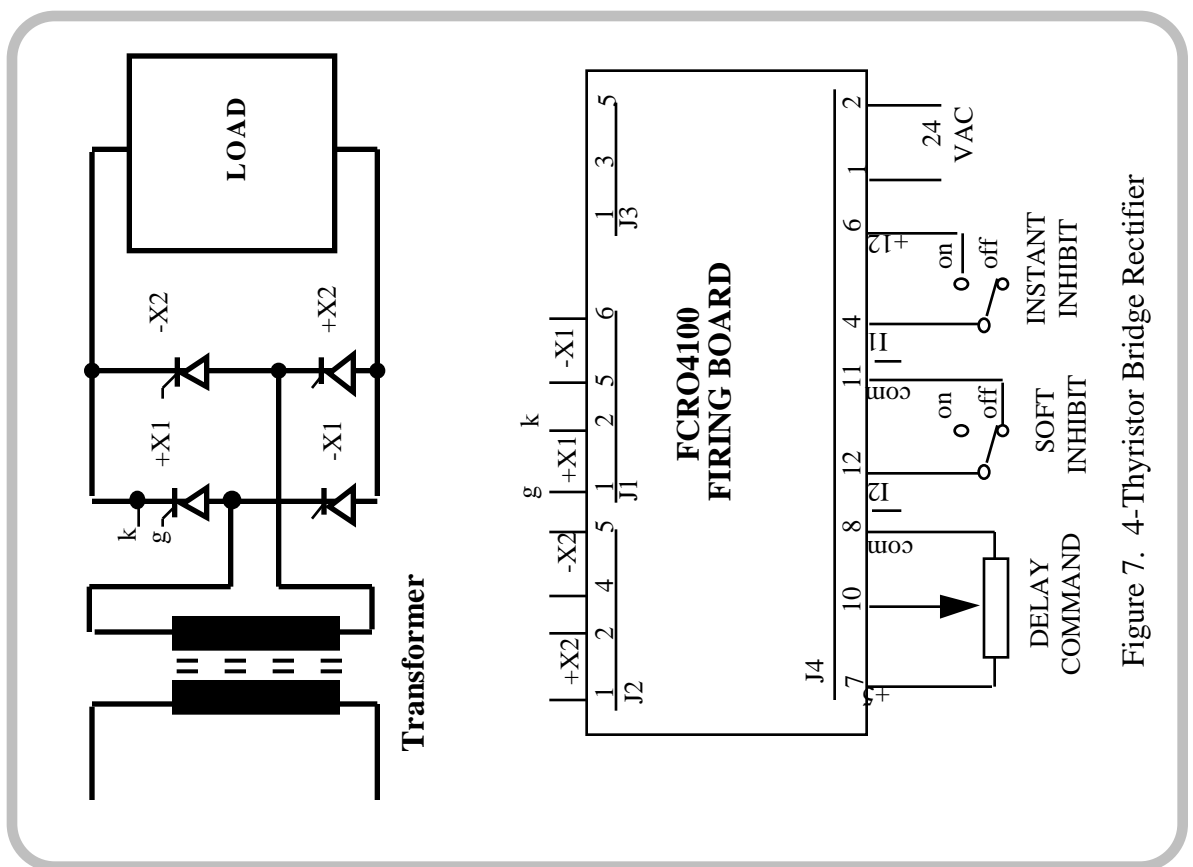


Figure 7. 4-Thyristor Bridge Rectifier

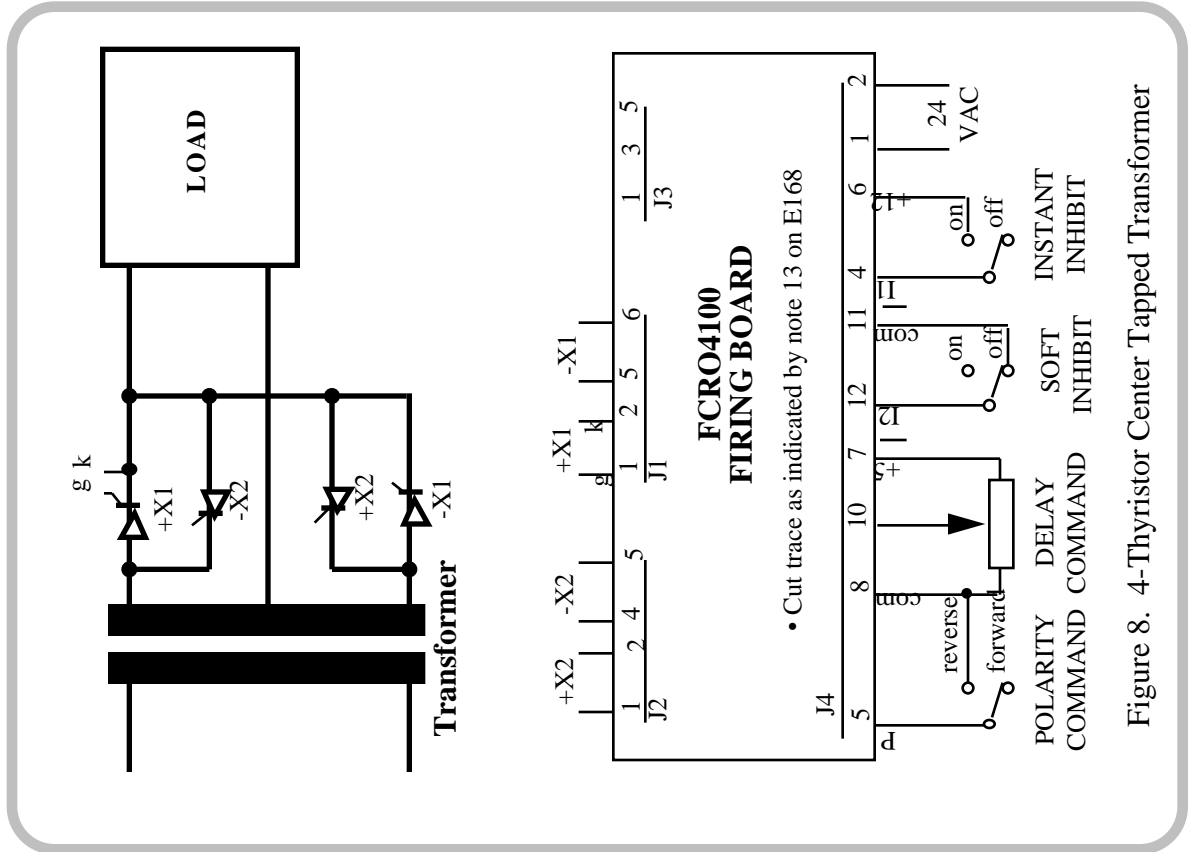


Figure 8. 4-Thyristor Center Tapped Transformer

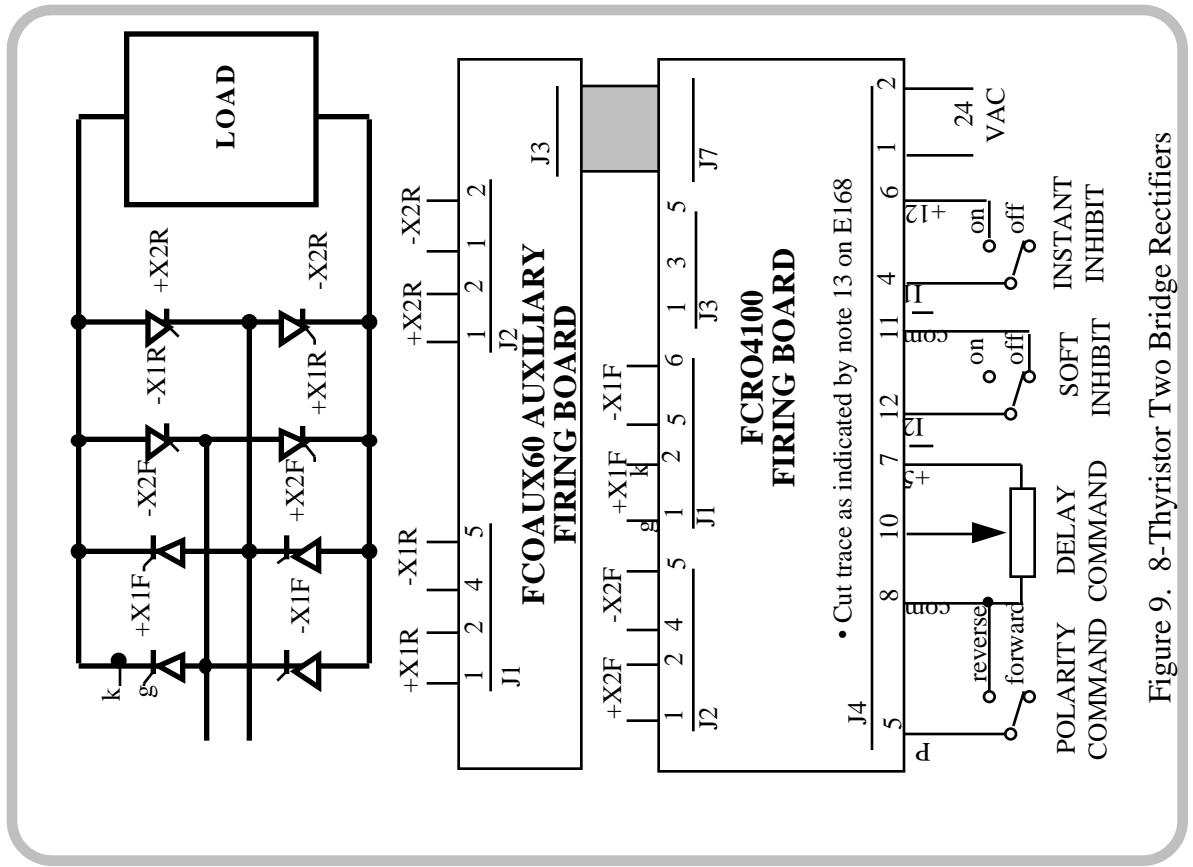


Figure 9. 8-Thyristor Two Bridge Rectifiers

INSTALLATION INSTRUCTIONS

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCR unit. An EP1031B (120/240Vac) transformer is assumed.

1. Remove board and connector package containing necessary interconnecting plugs and contact pins from packing.
2. The FCRO4100 board is provided with AMP Mate-N-Lok™ connectors on the board with mating plugs and contact pins contained in the separate connector package.
3. The contact pins supplied for interconnection with customer equipment are sized to be used with wire gauges from 14 AWG to 20 AWG. It is recommended that an AMP Service Tool II, or a quality "U" Barrel style, crimping tool for the proper wire gauge range be used for making these connections.
4. Refer to Figure 10 at this time for a brief description showing the location of the primary control and command connectors.
 - A. **J1** and **J2**, 6 position and 5 position connectors respectively, supply the actual gate signals to the customer's SCR's.
 - B. **J3**, 5 position connector, provides a connection point for input power to the onboard 24VA power supply. Boards are factory configured for use with 120/240Vac or 240/480Vac line voltages, as specified by the customer. This signal also provides the required phase reference signal to the control circuitry. As such, it must be in-phase with the power applied to the SCR's.
 - C. **J4**, 12 position connector, provides for customers SCR control signals "Gate Delay Command" and "Inhibit". This connector also provides instant SCR gating by utilizing the jumper contained in the connector package (see J4 note on Figure 10). It is also possible to power the board through this connector with externally sourced 24Vac.
5. The FCRO4100 firing board measures 7.5" wide x 6.0" high x 1.5" deep. The 4 (#8 SAE clearance) mounting holes provided measure 6.75" and 5.0" center to center. It is recommended that mounting spacers at least 1/4" long be utilized for panel mounting this device.
6. Mount the board mechanically. It is recommended that the board be physically mounted within 15" of the SCR's to be controlled to insure minimal inductive noise and positive gating of the SCR's.
7. Connection of the J1 and J2 Gate/Cathode control leads should be made at this time. It is recommended that the Gate and Cathode leads from the board to the SCR's be twisted pairs with at least one turn per inch to minimize inductive noise and possible false gating.
8. Connect the circuit board common at J4-11 or J4-8 to the chassis ground.

***WARNING** Check these connections very carefully before energizing the firing board. Improper or misconnections can short circuit SCR line voltage and result in product and/or customer equipment damage! If you have any questions concerning these connections please contact our customer support department for assistance.
9. Connection of the J4 Command and Control signals and/or closures should be made at this time. J4 also provides instant SCR gating by utilizing the jumper contained in the connector package (see J4 note on Figure 10).
10. Connection of board excitation voltage at J3 (see J3 note on Figure 10) should be made after careful examination of steps 7 & 8 above. NOTE: If the mains voltage is present, applying board power will gate SCR's after a short (50 msec.) delay.
11. Energize the board power supply. Verify that the green "PWR ON" LED indicator is on.
12. Increase the command signal input to the desired minimum input level or until the low

signal inhibit clears, whichever is higher. Then adjust the BIAS potentiometer, R6, to obtain the desired minimum SCR output.

13. Increase the command signal to the maximum input level and adjust the SPAN potentiometer, R7, as required to obtain the desired maximum SCR output.
14. Repeat steps 11 and 12 as required to obtain optimum system response.
15. Operate your controller as desired.

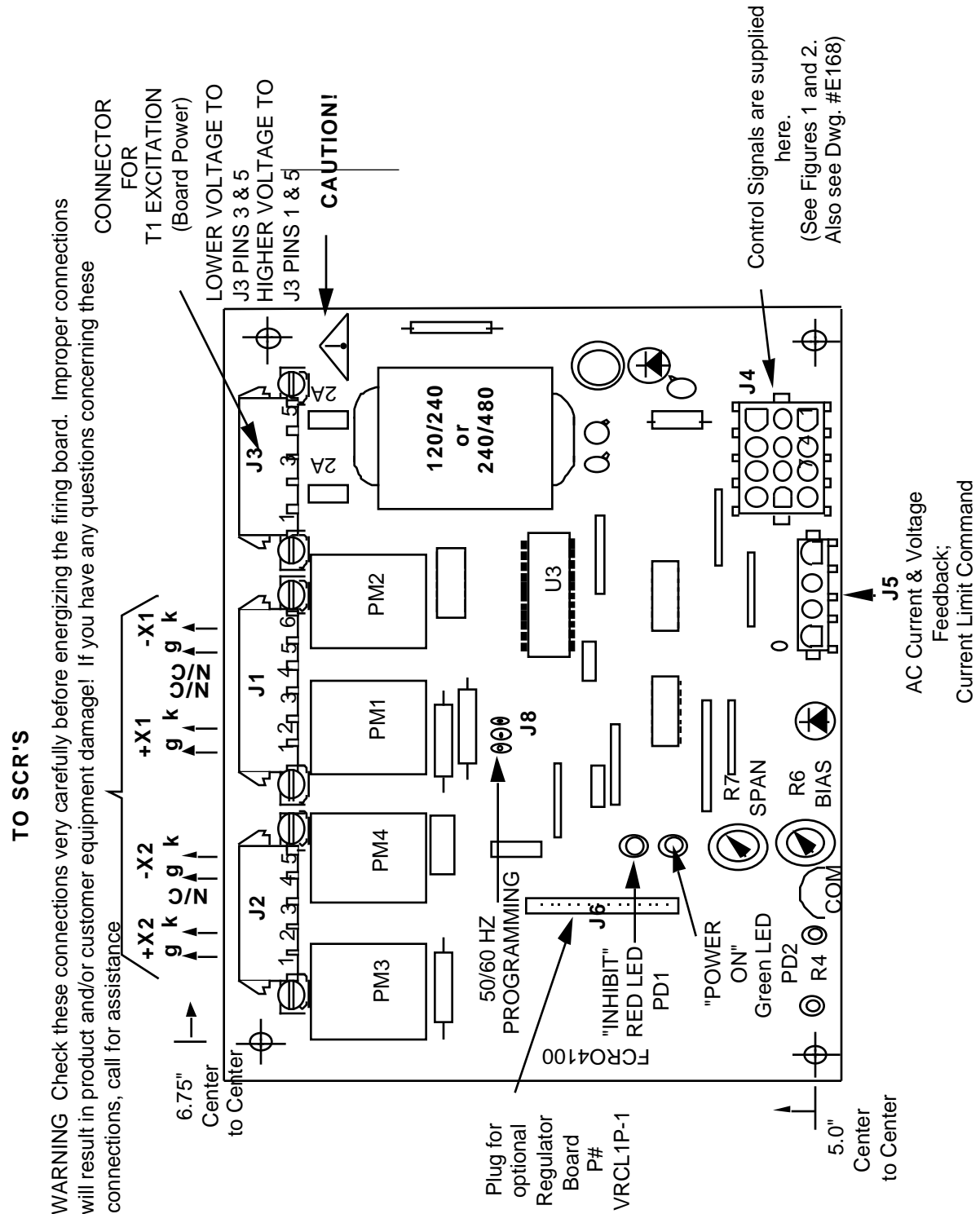


Figure 10. FCRO4100 Physical Drawing.

APPENDIX A

The following AMP Mate-N-Lok™ information is provided for your convenience. The part numbers referenced are valid as of this date and are currently used by Enerpro. However, these numbers are subject to change.

Description	AMP Number	Enerpro Stock Number
J1: 6-position Header (right angle)	640583-1	C2MNLRPH06
J1: 6-position Header (vertical)	350711-1	C2MNLVPH06
P1: 6-position Plug	640581-1	C2MNLPLG06
J2: 5-position Header (right angle)	1-350945-0	C2MNLRPH05
J2: 5-position Header (vertical)	640900-1	C2MNLVPH05
P2: 5-position Plug	350809-1	C2MNLPLG05
J3: 5-position Header (right angle)	1-350945-0	C2MNLRPH05
J3: 5-position Header (vertical)	640900-1	C2MNLVPH05
P3: 5-position Plug	350809-1	C2MNLPLG05
J4: 12-position Header (vertical)	350713-1	C2MNLVPH12
P4: 12-position Plug	350735-1	C2MNLPLG12
J5: 4-position Header (vertical)	350792-1	C2MNLVPH04
P5: 4-position Plug	350779-1	C2MNLPLG04
Contact Socket (20 - 14 AWG)	350552-1	N/A
Keying Plug	1-640415-0	C2KP94V0
Universal Crimp Tool	90287-1	N/A
AMP extraction Tool	458994-2	M2T458994

Table 2. AMP Mate-N-Lok™ Cross Reference