

ENERPRO	fjb,jt,jpm,ppd,lt	Eff. Date	Report Number R254
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1.0 INTRODUCTION

The PCA3DCE1175 is a phase controlled thyristor DC bridge assembly. This assembly is supplied to Original Equipment Manufacturers, or End Users, to incorporate into their own equipment. The design of this assembly makes it easy to install in new, as well as older equipment. Typical uses for this assembly would be in battery chargers, electrochemical processing and the front end converter for medical equipment. This assembly can be voltage and current regulated, either through the use of on-board shunts and pre-determined settings, or off-board command signals from an external source. This assembly is comprised of the industry standard circuit boards, the FCOG6100 3Ø Thyristor Firing Board, ISOVLCL-1 Isolated Voltage and Current Regulator Board and the TSB-6 Transient Suppression Board.

2.0 SPECIFICATION

Part Number:

- PCA-3-DC-FC-216-64-092-400-E1175

Environment:

- Ambient Temperature: 0°C to 45°C

AC Power:

- Voltage Sequence: may be a, b, c or a, c, b
- Frequency: 50/60 Hz
- AC Voltage: 380Vac

Thyristor Modules:

- Rated average current (Both thyristors) 95A @ 85°C case temperature
- Rated 1 cycle peak current (each thyristor) 2000A
- Blocking Voltage 1600Vac
- dV/dt 1000V/μs
- dI/dt (repetitive) 100A/μs

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Circuit Board Power:

- Voltage 120/240Vac
- Rating 24VA maximum

Converter Output:

- Voltage 0Vdc to 540Vdc
- Current 50A dc
- Ripple Frequency 360Hz @ 60Hz, 300Hz @ 50Hz input

Control Law:

- Voltage limit The regulated converter is in the voltage limit mode when:

$$I_{\text{setpoint}} > (E_{\text{setpoint}} - E_{\text{load}} - \text{CEMF}) / R_{\text{load}}$$

- Current Limit The regulated converter is in the current limit mode when:

$$E_{\text{setpoint}} > (I_{\text{setpoint}} * R_{\text{load}} + E_{\text{load}} + \text{CEMF})$$

Voltage Isolation:

The low level control circuits are isolated from the AC supply and DC load as follows:

- From the AC supply by three 2.00Mohm phase reference sensing resistors.
- From the AC supply and DC load by the 4500Vac (1 minute) rating of the six gate pulse transformers.
- From the DC load by the 1500Vrms (continuous) rating of the AD202KN feedback isolation amplifiers.

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- From the 120/240Vac circuit board supply by the 2500Vac (1 minute) rating of the firing board power transformer.

Feedback Signals:

- Rectifier Voltage: From the voltage attenuator on the assembly.
- Rectifier Current: From 50A:50mV shunt on the assembly.

Voltage and Current Limit Commands:

The limit commands are set by onboard potentiometers, or by external 0 to 12 Vdc signals. Note: these command signals can be from just about anywhere, a PLC (0-10 Vdc) or external potentiometers are a few examples.

3.0 INSTALLATION

The assembly is designed to be installed through the wall of an electrical cabinet in such a way as to allow the cooling fins of the heat sink to be outside for optimal heat dissipation. If it is not possible to mount the unit in such a way that the heat sink fins are outside, then a moderate flow of cooling air will be required in the cabinet with a way to exhaust it out to the outside environment.

Mating connectors and pins are provided for each of the board mounted connectors. Care must be exercised when installing these pins and connectors to assure that various control signals are properly attached. Refer to connection diagram E1175 for proper hook up.

4.0 FIRING BOARD OPERATIONAL INFORMATION

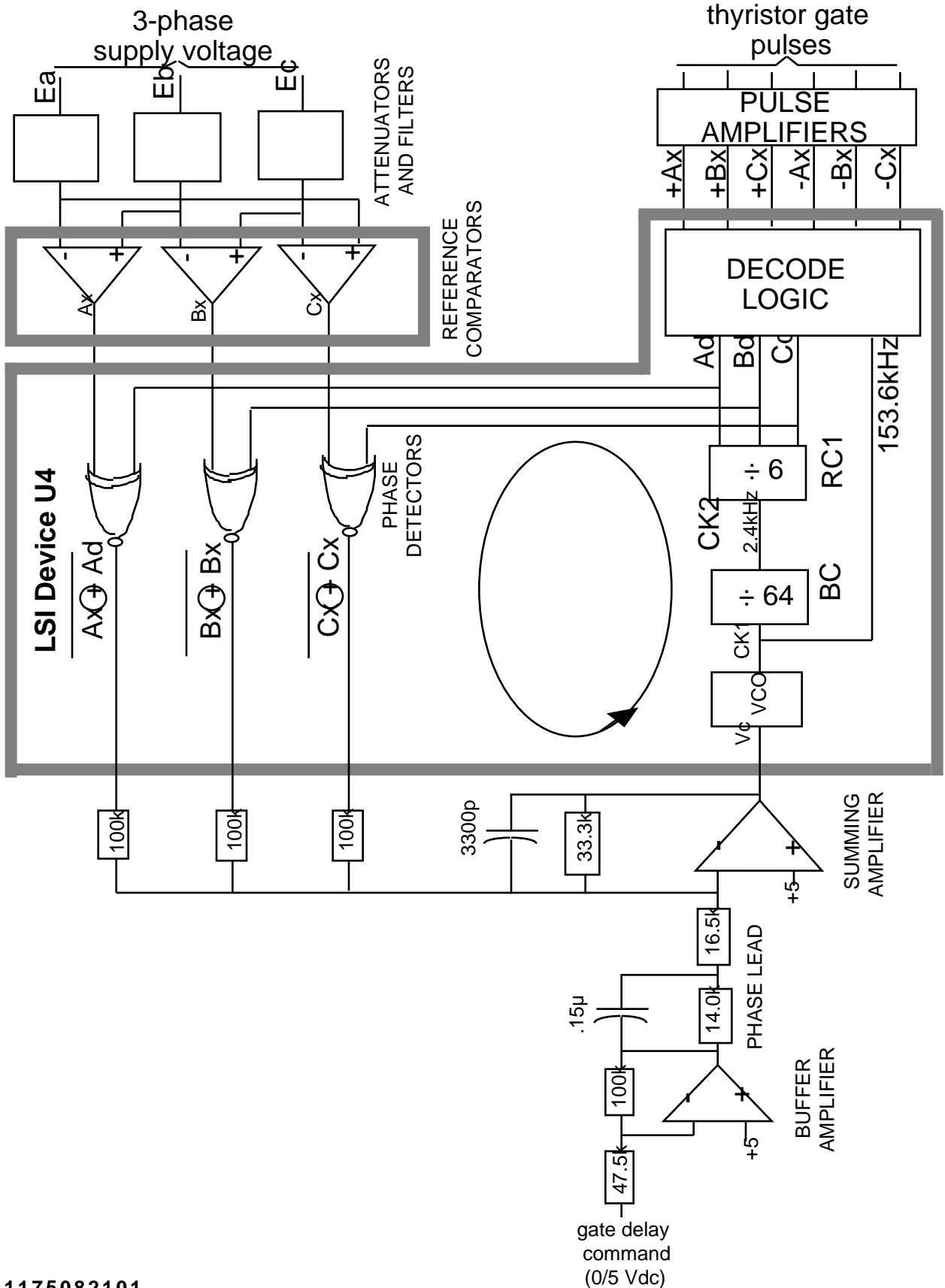
The FCOG6100 6-pulse firing board is an industry standard, of which approximately 30,000 are in service in various industrial applications. Figure 1 shows a simplified block diagram of the gate delay determinator.

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Instant Gate Inhibit

The FCOG6100 board is commanded on and off by using the instant inhibit circuit. This connection, J3-4, is pulled low by RN5-4 when a positive command is not applied. The application of a positive command will cause DN1-3 to become reverse biased and U6-12 to increase to the output of U6-1 (5.0Vdc). This value is above the 1.3Vdc threshold at U6-13 and will cause the inhibit to clear. The thyristors will then be gated at the commanded angle.

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Figure 1. 6-Pulse Gate Delay Generator Equivalent Circuit

Phase References

The phase references for the phase locked loop (PLL) delay angle generator are derived from the three phase ac supply voltages. These voltages are applied to the firing board at J2. The supply voltages are processed by resistive attenuators, low pass filters, phasor addition circuitry, and differential comparators.

The time constant of the low pass filter is selected to give a lagging phase shift of $\theta = 60^\circ$ at the 60Hz operating frequency. A phasor addition technique adds a 60° phase lead, giving an adjusted reference delay phase shift at 60Hz of 0° .

The three attenuated and filtered reference signals are applied to three voltage comparators. These comparators are contained in device U7 (ref. FCOG6100 schematic diagram E128). Additional circuitry is contained in U8 to modify the comparator input signals to give correct reference phasing when the sequence of the ac power is reversed.

Phase Loss Inhibit

A phase loss detection circuit operates to instantly inhibit thyristor gating if the mains phase balance is abnormal or, in the extreme case, if one phase voltage is missing. Gating is enabled when the proper phase balance is restored: gating initiates at the maximum delay angle and ramps to the commanded angle in approximately 1.5 seconds.

The reference comparator outputs are summed through 47.0k resistors and filtered by C28 (0.033 μ F). This produces a triangular waveform which is applied to comparators located in U5. A resistor divider circuit sets the upper and lower phase loss thresholds for U5. In the case of a large phase unbalance, or a loss of phase, the summed comparator waveform becomes distorted. This distortion causes the waveform to cross either the upper or lower threshold and toggles the comparator output. The low comparator outputs are then applied to the phase loss indicator, LBCCIB-1 (through interconnecting wiring), and the soft-start/stop circuit. The soft-start/stop circuit capacitor, C3, will instantly discharge causing the board to instantly inhibit (U6-12 will

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be pulled below the U6-13 threshold of 1.3Vdc) and the delay angle to increase (DN1-7 and R53 allow the soft-start/stop circuit to pull the buffer amplifier summing junction low. This causes the output of the buffer amplifier to increase in order to maintain 5.0Vdc at the inverting input. This, in turn, causes the delay angle to increase. When the phase loss clears, capacitor C3 will charge through R44, DN1-4, and RN5-5. Charging capacitor, C3, will clear the inhibit and allow the delay angle to ramp to the commanded angle.

Three Phase Phase Locked Loop

The reference comparator outputs, designated as Ax, Bx and Cx in Figure 1, are applied to three EX-OR phase detectors in LSI device U4. The other three inputs to the phase detectors are produced by ring counters in LSI device U4, as described below.

The outputs of the three phase detectors in U4 are summed with three 100k resistors and applied to the inverting input of the summing amplifier. The output of the summing amplifier sets the frequency of the voltage controlled oscillator (VCO). This clock signal is designated as CK1 in Figure 1. The clock frequency is 384 (= 6 x 64) times the mains frequency when the PLL is in lock. A ÷64 binary counter (BC) operates on CK1 to produce a second clock signal, CK2, which is 6 times the mains frequency. A ÷6 ring counter (RC1) outputs the three delayed phase references for the EX-OR phase detectors in U4.

Steady-State Transfer Function

The 0.0Vdc/5.0 Vdc gate delay angle command signal from the regulator board is amplified by a factor of $-100/47.5 = 2.11$ in the buffer amplifier and applied through a pair resistors to the inverting input of the summing amplifier. The output voltage of the summing amplifier is at a constant average level (in the range of 4.5 Vdc to 5.5 Vdc) when the PLL is in lock. This enforces the requirement that a change in the output of the buffer amplifier be matched by a proportional and opposite change in the average voltage at the outputs of the six EX-OR phase detectors. The factor of proportionality is the ratio of the control signal input resistance (30.5k) to the effective value of the resistance's that sum the phase detector outputs (= $100/3 = 33.3k$). Since a 180° change in the phase angle between the mains voltage

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phase references Ax ---- Cx and the delayed phase references Ad ----- Cd corresponds to a 12 Vdc change in each EX-OR output, a change in the delay angle command, SIG , results in gate delay angle change , of:

$$\begin{aligned} / \text{ SIG HI} &= (100/47.5) \times (30.5/33.3) \times (180/12) \\ &= 28.92^\circ/\text{V} \end{aligned}$$

Gate Command Decoding

The delayed reference signals Ad, Bd and Cd are applied to decoding circuits in LSI device U4 to produce the required 6 gate pulse command signals. These signals are precisely spaced by 60° and shifted in phase from the line-to-line voltage zero crossings by the delay angle α . The gate pulse profile is a "picket fence" of 128 pulses having a 50% duty cycle and a pulse width of 3.26µsec. This profile is produced by decoding circuitry which ANDs the 153.6kHz clock, CK1, with the 60Hz outputs of the ring counters in U4. Since the gate pulse carrier is phase-locked to the mains frequency, the first pulse in the gate pulse train always has a full 3.26µsec pulse width.

Gate Pulse Amplifier

Circuitry shown in drawing E128 (and Figure 2, below), consisting of transistor array U3, resistors R3 - R6, capacitors C11 - C13, and gate pulse isolation modules PM1-PM6 amplify and shape the thyristor gate current pulses. Each pulse module consists of a 1.67:1 ratio pulse transformer tested for 4500Vrms isolation, two secondary diodes, noise suppression resistors across the primary and across the gate drive output, and a fuse in series with the output.

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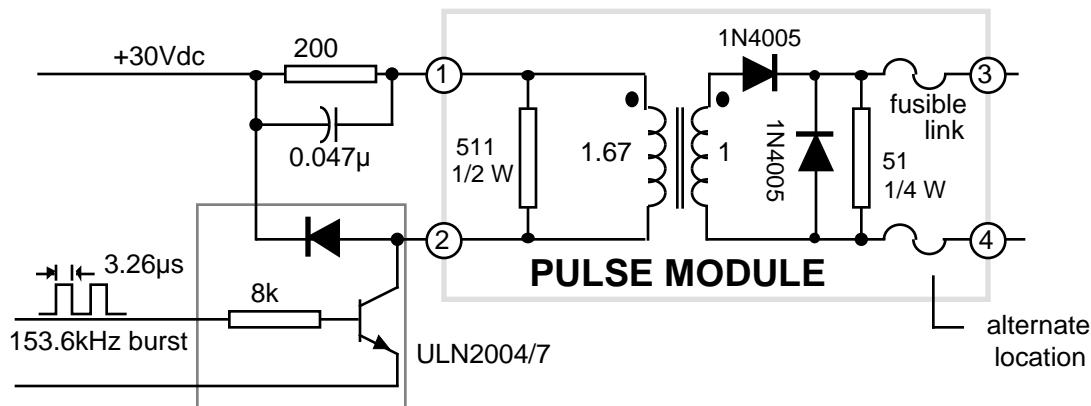


Figure 2. Gate Pulse Amplification Circuitry

5.0 CURRENT/VOLTAGE REGULATOR BOARD OPERATION

The ISOVLCL-1 regulator board responds to voltage command signals and adjusts the gate firing phase angle to regulate load voltage or current (automatic crossover).

The regulator board performs the following functions:

- Isolation of the voltage and current feedback signals from the control circuits.
- Pre-filtering and pre-amplification of the current feedback signal.
- Pre-filtering of the voltage feedback signal.
- Absolute value functions for the current and voltage feedback signal's.
- Low pass post-filtering of the voltage and current feedback signals.
- Limit amplification of the current and voltage feedback signals.
- Diode-OR circuit for automatic crossover between voltage and current limiting.
- Over-current comparator operating on the pre-filtered and pre-amplified current signal.
- Soft-start in response to an enable command.
- Load current and load voltage readout signal's.

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Voltage Limit Channel

The attenuated rectifier output signal is processed by a single pole low pass filter ($T = .35$ sec) and unity gain isolation amplifier to form a feedback signal referenced to circuit board common. This signal is then amplified by a x2 gain precision rectifier and applied to the input of a limit amplifier. The limit amplifier has a gain of 4.6 V/V and the low pass filter time constant of .01 sec.

The limit amplifier responds to the difference between the voltage feedback signal and the voltage limit command. When this difference is positive, the voltage limiter output decreases from a quiescent level of approximately 14 V. The limit amplifier output is coupled via diode DN1-3 to pull-up resistor RN5-1. The common connection of RN5-1 and the anodes of diodes DN1-3, DN1-4 and DN1-5 responds to that diode which is conductive; in this case, voltage limit diode DN1-3. The diode common point voltage is amplified by a x2 gain non-inverting amplifier and applied through coupling resistor R28 to the FCOVF6100 firing board. This is the SCR gate delay command voltage, designated as SIG HI in Figure 3.

Current Limit Channel

The rectifier output current is sensed by a 50 mV shunt, low pass filtered ($T = .00022$ sec.) and preamplified with a gain of 20. The result is a load referenced wideband current feedback signal having a full scale level of $20 \times .05 = 1.0$ Vdc. The amplified signal is processed by a unity gain isolation amplifier to form a current feedback signal referenced to circuit board common. This signal is then amplified by a x2 gain precision rectifier and applied to the input of a limit amplifier. The limit amplifier has a gain of 4.6 V/V and the low pass filter time constant of 0.33 sec.

The current channel limit amplifier and its associated coupling diode DN1-5 operate in the same manner as the voltage channel described above. If the current channel limit amplifier output is at a lower voltage than the voltage channel limit amplifier, the current feedback channel dominates and forms the SCR gate delay signal into the firing board.

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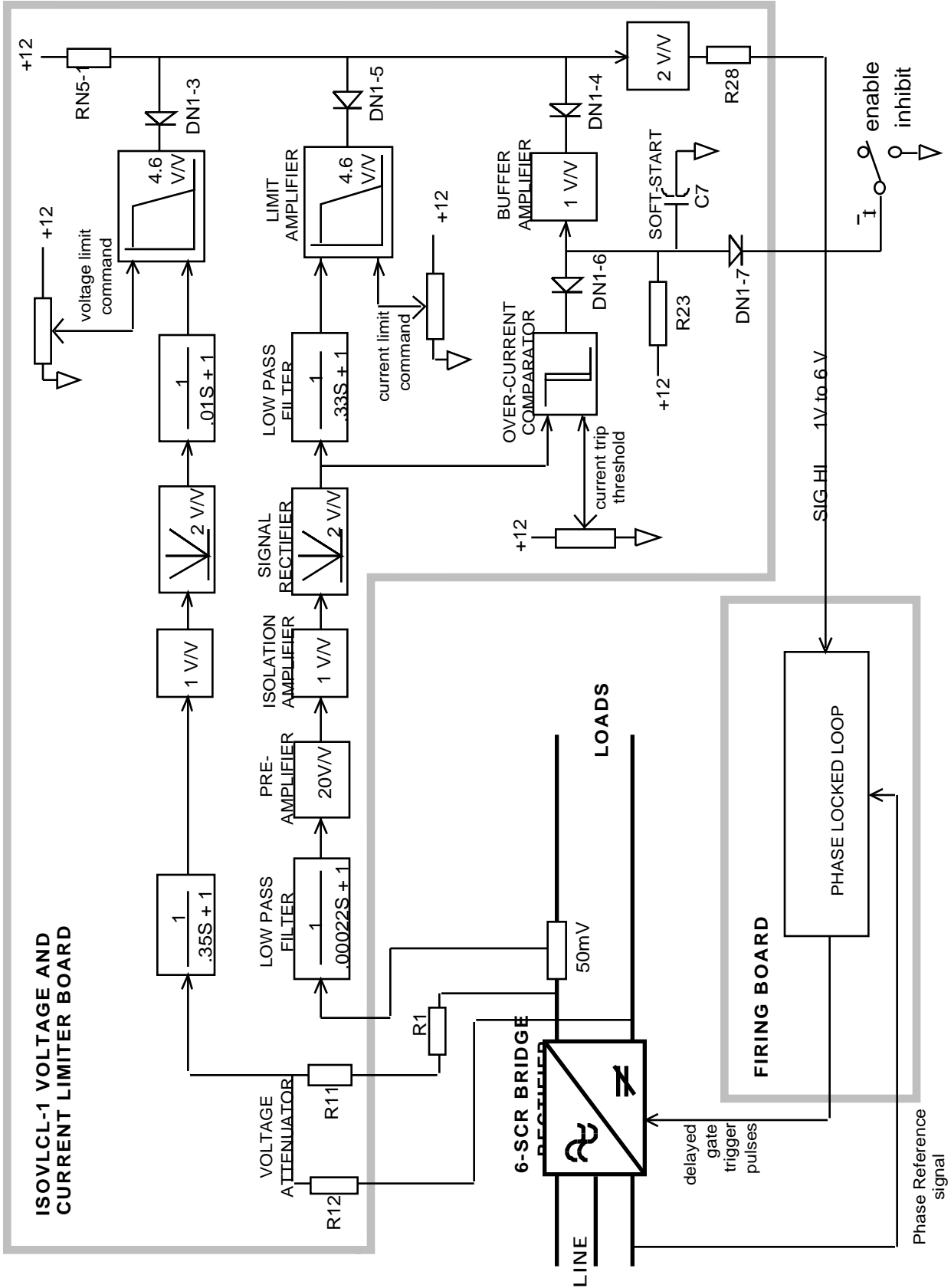
Current Trip & Soft-Start Circuitry

The overcurrent comparator circuit responds to the current feedback signal at the output of the precision rectifier and to a current trip threshold voltage obtained from a board mounted trimpot. When the current feedback signal exceeds the trip threshold, the comparator output goes low and discharges soft-start capacitor C7. The C7 voltage is buffered and coupled by diode DN1-4 to the common connection of RN5-1, the anodes of DN1-3, DN1-4 and DN1-5 and the input to the x2 gain amplifier. The SIG HI input to the firing board decreases to a low voltage in response to the overcurrent event, thus retarding the SCR gate delay angle and reducing the load current to a value less than the current trip threshold.

Reduced load current causes the output of the overcurrent comparator to snap back to the positive supply voltage rail, thus allowing the soft-start capacitor C7 to recharge through resistor R23. If the rectifier load fault which caused the overcurrent persists, the current trip level will again be exceeded and current will again be reset. This cycle will continue until the load fault is removed.

The soft-start capacitor C7 will be discharged, thereby reducing the rectifier output current to zero through the process described above, by a logic zero condition applied to the cathode of diode DN1-7. This inhibit signal is designated as I in Figure 3.

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Figure 3. ISOVLCL-1 Block Diagram

6.0 MAINTENANCE

Enerpro boards and assemblies are designed for long life in rugged environments. Generally there is no maintenance required other than to check the cooling fins of the heat sink for cleanliness from time to time, depending on the environment.