Twelve-Pulse Converter With Auto-Balance and Integrated Magnetics Cuts THD

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Line-commutated-thyristor converters and controllers remain a viable way to convert and control three-phase power. They can achieve this because of the thyristor's inherent advantages: very high short-circuit ruggedness, high voltage device availability and motor-winding-friendly switching characteristics. However, increasingly stringent Total Harmonic Distortion (THD) specifications are shifting industry demand from traditional six-pulse converters to the more sophisticated 12-pulse designs.

Twelve-pulse conversion reduces the harmonic demand on the ac supply by virtually eliminating the 5th and 7th current harmonics. Proven industry standard 12-pulse thyristor firing circuits contribute to the practicality of 12-pulse conversion. However, the cost of the magnetics remains a major barrier to acceptance. Automatic balancing of the phase shift transformer loads and the combined interphase transformer and dc choke described below promise to diminish these barriers.

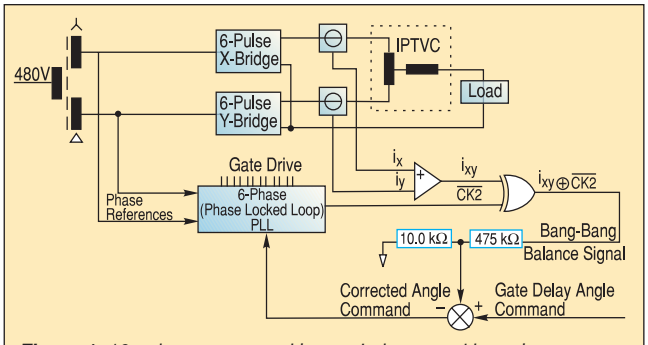

Figure 1. *12-pulse converter with auto-balance and interphase transformer/virtual choke.*

Phase Shift Transformer Imperfections

The parallel 12-pulse converter (*Figure 1*) consists of two 6-pulse thyristor bridges powered from a wye/delta secondary isolation transformer to provide phase shifted ac power to each bridge. Ideally, the two sets of three-phase voltages are equal in amplitude and phase shifted by 30°. In practice, unequal leakage inductances and the inability to achieve the ideal EMBED Equation.DSMT4 :1 turns ratio between delta and wye windings causes a voltage imbalance and a deviation from 30° phase shift. As a result, there are unbalanced currents from the paralleled bridges. This leads to unequal heating of the transformer secondaries, imperfect harmonic cancellation and residual 360 Hz ripple voltage in the converter output.

An auto-balance method provides active control of the 30° group thyristor gate delay angle to equalize the two bridge currents at all ac output levels. The circuit requires two current feedback signals, labeled ix and iy (*Figure 1*). These current feedback signals are scaled to about 1.0V at rated current. The current signals are applied to a voltage comparator to create the logic signal, Ixy. The Ixy signal is applied along with the 360 Hz clock signal CK2 to the input of the EX-OR gate. The attenuated EX-OR output is summed as a bang-bang balance control signal with the gate delay command at the input to the Phase-Locked Loop (PLL). The balance control signal increases the gate delay angle of the high current bridge and reduces the gate delay angle of the low current bridge. The balance signal is scaled to produce a maximum deviation in the group delay angle of ±2°. The auto-balance circuit reduces the difference in the two bridge currents to typically 10% or less of the total dc output current.

IPTVC, the interphase transformer/virtual choke, serves two functions. First, it provides the differential-mode inductance necessary to buffer the instantaneous dc output voltages of the paralleled six-pulse bridges. Additionally, the IPTVC eliminates the need for a separate dc choke by providing the common-mode inductance necessary to reduce the DC link ripple voltage and current to acceptable levels.

The IPTVC is created by winding coils on the outer legs of a three-leg core. The coupling between the coils on the outer legs provides the differential-mode inductance while the shunt flux path of the center leg creates the common-mode inductance.

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