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Operating Manual: FCOG61BP Six-SCR General Purpose Bipolar Gate Firing Board

Introduction

This manual describes the salient features and specifications of the FCOG61BP firing board, including typical firing circuit signal waveforms and a checkout procedure.

Product Description

1.0 Application

The FCOG61BP allows simple implementation of reversing rectifiers and sequence-reversing AC controllers. The firing board responds to a voltage or current delay angle command signal (SIG HI) to produce a delayed set of six isolated, 60°-spaced high-current SCR gate firing pulses. A polarity transition input allows users to switch between two sets of six isolated gate drive outputs; one designated as the forward direction and the other as the reverse direction.

2.0 ASIC-Based Firing Circuit

All firing circuit logic is contained in a custom 24-pin ASIC. Additional detail on the firing circuit theory is contained in a separate engineering society paper[1].

3.0 Board Mounted Connectors

The firing board is connectorized to simplify maintenance and troubleshooting (see schematic drawing E1535).

3.1. Gate-Cathode Connectors

The SCR gate-cathode connect via 8-position Mate-N-Lok™ right-angle connectors[2] J1 and J4 for the forward direction and J2 and J3 for the reverse direction. The connectors are keyed to prevent incorrect installation of the mating plugs. When the SCRs are arranged as antiparallel bridge rectifiers (see Figure 1), connector J1 accesses the gates and cathodes of the three SCRs having line-connected cathodes in the forward bridge. Connector J2 accesses the gates and cathodes of the three SCRs having line-connected cathodes in the reverse bridge and provides the ac mains reference signals when they are obtained directly from the cathodes of the SCRs. Connector J3 accesses the gates and cathodes of the three SCRs having load-connected cathodes in the reverse bridge. Connector J4 accesses the gates and cathodes of the three SCRs having load-connected cathodes in the forward bridge.

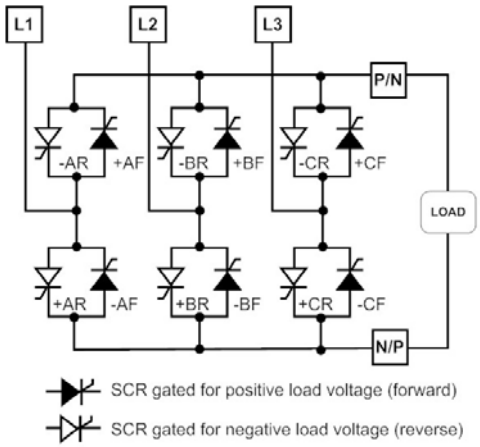

Figure 1. SCR Connections for a typical reversing rectifier application

[1] Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.
[2] Vertical connectors are available upon request.

3.2. Control Signal Connector

The firing board connects to the gate delay command and inhibit controls through a 12-position Mate-N-Lok™ connector J5. This connector also accesses the 24 Vac and 30 Vdc lines.

3.3. Power Supply Excitation

The FCOG61BP is powered with 24 Vac or 30 Vdc applied to J5 pins 1 and 2 or 3 and 11, respectively.

3.4. Onboard Phase References

Phase references are normally derived directly from the SCR cathode connections on J2. An RN65 resistor in each pulse module forms, with RN11, a resistive attenuator. These signals provide the phase reference information required by the analog delay angle determinator. Table 1 lists the part numbers for the pulse modules and the associated internal phase attenuation resistor values for different ac line voltage ranges.

Table 1. Pulse Module Selection

Enerpro Part Number	Internal Phase Attenuation Resistor	Typical AC Mains Range
EP1024-0	None	N/A – Configured for external references
EP1024-1	2.00 MΩ	300 – 600 Vac
EP1024-2	511 kΩ	150 – 300 Vac
EP1024-3	200 kΩ	30 – 150 Vac

3.5. Offboard Phase References

In certain applications, the ac mains voltage may not be present at the SCR cathodes or the ac voltage may go to zero during load faults[3]. In these cases, or when galvanic isolation is required between power and control circuits, external phase reference voltages are applied through optional Mate-N-Lok™ connector J7.

DO NOT APPLY THE UNATTENUATED AC MAINS VOLTAGE AT J7. Applying the full ac mains voltage at J7 will result in severe board damage and void any warranty on the product. You must connect series attenuating resistors between J7 and the ac mains according to the voltages listed in Table 1.

3.6. Phase Reference Test Signal Input Connector

For low-power testing, users may connect low-level (5 V_{PP}) three-phase test reference signals to the three-position MTA connector J6 (functionally equivalent to J7).

3.7. Auxiliary Firing Board Connectors

To facilitate the use of Enerpro auxiliary firing boards for high voltage or parallel SCR applications, the gate firing signals are brought out on two eight-position MTA connectors J8 and J9. Connector J8 provides the forward gate firing signals while J9 provides the reverse firing signals; J8 and J9 also connect to 30 V and the board common.

4.0 Gate Delay Command

The delay command signal, SIG HI, may be configured either as a 4 to 20 mA current command or one of several voltage commands. The default SIG HI voltage range is 0 to 5 V. The input resistance presented to the delay command signal SIG HI is determined by resistor R30; this value is 10.0 kΩ when the control signal is designated as a control voltage. The buffer amplifier resistance table below lists the resistor values associated with different command signal levels. See also schematic diagram E1535.

[3] For example, in a 6-SCR interphase transformer converter or an arc welder converter.

Table 2. SIG HI Range vs. Buffer Amplifier Component Values

SIG HI Range		**Resistance** (in kΩ unless noted)					Zener Voltage
	R13	*R18*	*R24*	*R25*	*R26*	*R30*	*D10*
0 - 5 V	32.4	1meg	130	46.4	100	10.0	6.2
0.85 - 5.85 V	32.4	1meg	196	46.4	100	10.0	6.2
0 - 10 V	32.4	374	1meg	90.9	100	10.0	11
0 - 2 V	32.4	1meg	78.7	46.4	274	10.0	6.2
4 - 20 mA	32.4	1meg	130	46.4	100	249Ω	6.2

5.0 Gate Inhibits

SCR gating is enabled by connecting either the instant inhibit, $\overline{I_1}$, to 12 V or by disconnecting the soft inhibit, $\overline{I_2}$, from ground. These signals are located at J5 pin 4 and J5 pin 12, respectively.

The instant inhibit signal $\overline{I_1}$ is normally pulled to ground RN9A (1.50 kΩ). The user connects the $\overline{I_1}$ signal to 12 V to enable firing. This arrangement ensures that SCR gating is inhibited if plug P5 is inadvertently disconnected. A jumper may be installed between pins 4 and 6 of P5 to hold $\overline{I_1}$ at 12 V at all times in applications where the instant inhibit is not needed.

The soft inhibit signal $\overline{I_2}$ is normally pulled to 12 V through RN9B (1.50 kΩ). The user grounds $\overline{I_2}$ to soft-stop SCR firing. In this mode, the delay angle is ramped from the setpoint value determined by SIG HI to the largest angle possible, after which firing is completely inhibited. This is termed the soft-stop shutdown mode. When user opens the connection at $\overline{I_2}$, gating is enabled with the delay angle set to the maximum limit. The delay angle then ramps to the value determined by SIG HI. The soft-stop and soft-start time constants are independently configurable via two timing resistors (R28 and R27 respectively) and capacitor C17.

6.0 Phase Loss Inhibit

The FCOG61BP's phase loss circuit instantly inhibits SCR gating if the mains voltage phases are grossly imbalanced or, in the extreme case, if one or more phase voltages are missing. This feature also eliminates the possibility of erratic response associated with voltage imbalance or transients when the three-phase mains are initially connected to the SCRs. After any phase loss fault, the board soft-starts when the fault is cleared. The Revision C phase loss circuit is immune to line frequency variations and transient voltages on the SIG HI line.

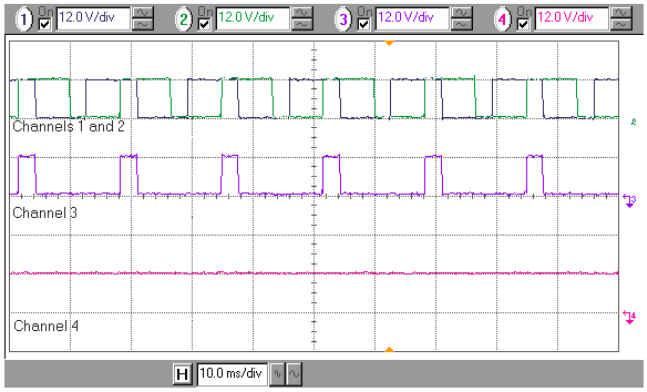

Figure 2. Phase Loss Circuit Signals – No Phase Loss[4]
Channels: 1. Digital A Phase Reference Signal, U4 P11
2. Digital B Phase Reference Signal, U4 P9
3. A and B logic signal, TP9
4. $\overline{PL}$ Signal, U4 P1

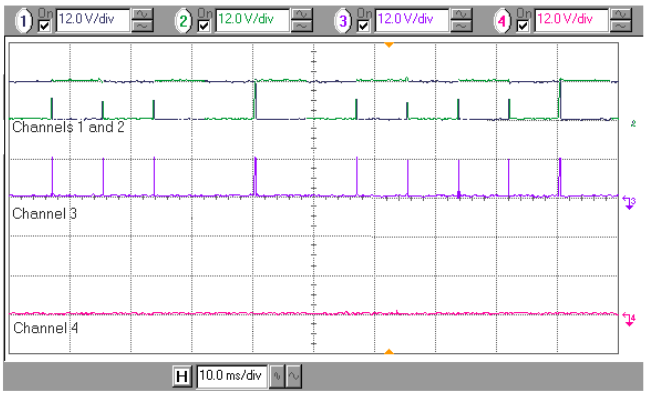

Figure 3. Phase Loss Circuit Signals – Phase Loss
Channels: 1. Digital A Phase Reference Signal, U4 P11
2. Digital B Phase Reference Signal, U4 P9
3. A and B logic signal, TP9
4. $\overline{PL}$ Signal, U4 P1

7.0 Phase Reference Shift Selection

First-order RC lowpass filters formed by RN10 and capacitors C31-33 shift each mains phase reference by 0° for controller applications or by -30° for converter applications.

For 30° lagging references as in Figure 4, C31-33 are 0.033 µF film capacitors and RN10 is a 120 kΩ, three-position, isolated SIP resistor network.

[4] All waveforms contained in this document were obtained with the FCOG61BP revision C firing board connected to 240 Vac, 60 Hz, balanced 3-phase mains. The time base of each screenshot has been calibrated for phase measurements as noted at 60 Hz. All component designations refer to drawing E1535, revision C.

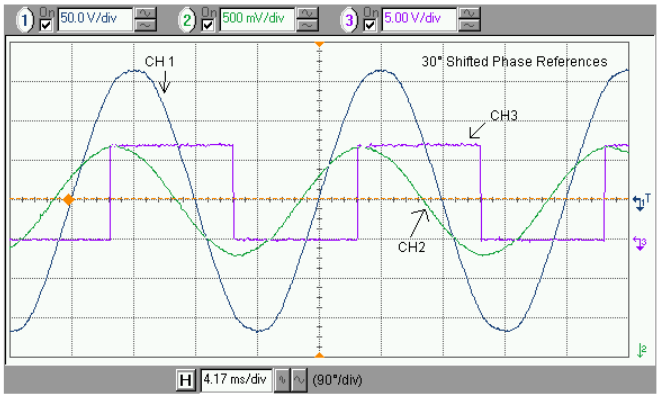

Figure 4. Thirty-degree shifted phase references, Phase A
Channel: 1. Phase A Line-to-Neutral Voltage
2. Attenuated and Filtered Mains Voltage at RN10-1
3. Reference Comparator Output, TP5

For 0° references as in Figure 5, 0.01 µF film capacitors may be installed with RN10 = 120 kΩ. Alternatively, 0.033 µF film capacitors may be used with a 33 kΩ resistor network installed at RN10 for 0° shifted references. This is an optimal scheme if the same firing board may be used to fire controllers or converters, as the user may then simply change RN10 (typically supplied in a socket in this case) to achieve the required phase shift.

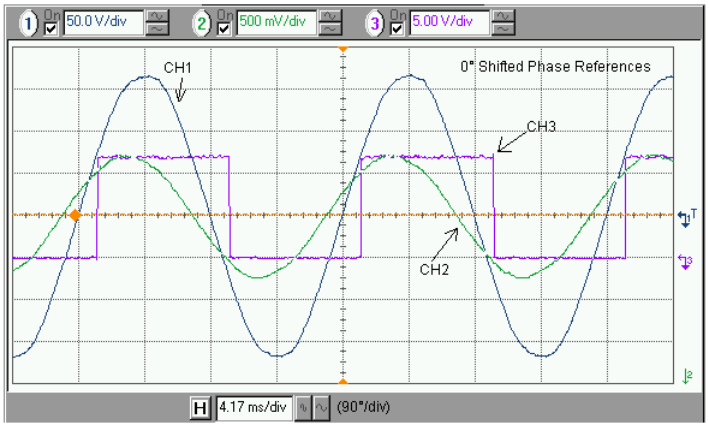

Figure 5. Zero-degree shifted phase references, Phase A
Channel: 1. Phase A Line-to-Neutral Voltage
2. Attenuated and Filtered Mains Voltage at RN10-1
3. Reference Comparator Output, TP5

8.0 Gate Pulse Profile Selection

Jumper JU1 enables gate pulse profile selection: when installed, the pulse profile is two 30°-wide bursts; when omitted, the profile is a single 120°-wide burst. In both cases each burst has an initial high-amplitude pulse (15 V open circuit, 2 A short-circuit) followed by lower amplitude

sustaining pulses (7 V open circuit, 0.5 A short circuit), ensuring continuous SCR conduction over the required period.

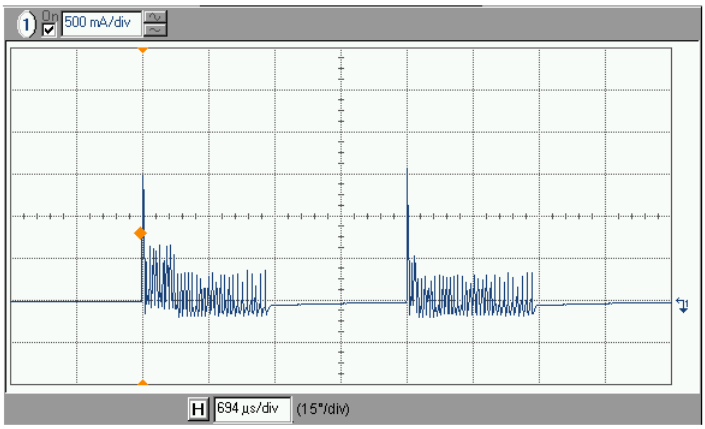

Figure 6. 2-30° Gate Pulse Profile (Into 1Ω)[5].

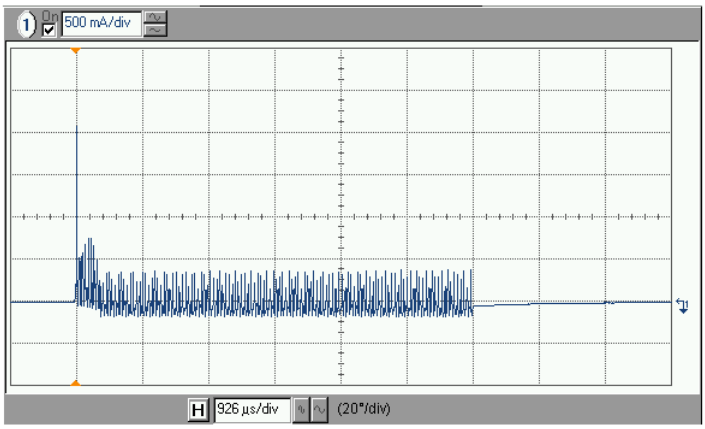

Figure 7. 120° Gate Pulse Profile (Into 1Ω).

[5] Current waveforms obtained using a Pearson model 2877 current transformer with 4 primary turns. The current transformer is terminated by the scope's 1.0 MΩ input impedance.

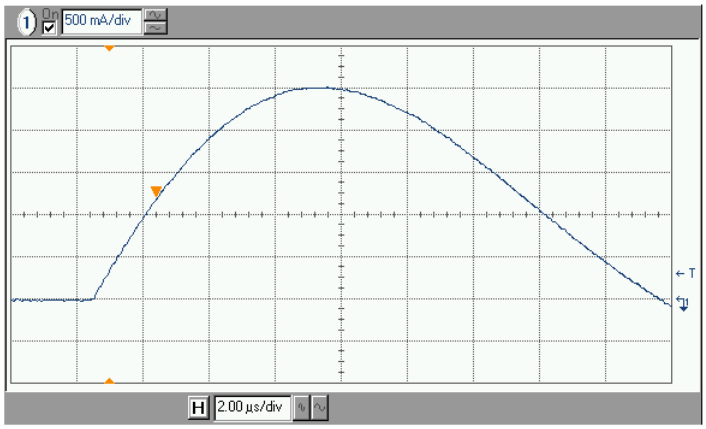

Figure 8. Initial pulse profile detail (Into 1Ω).

The firing circuit uses a phase-locked loop (PLL) to lock the firing pulses to the three mains phases. A series of counters divide the PLL's oscillator output and a decoder section then generates six 120°- wide delayed logic signals. For the 120° single burst profile, the 120°-wide delayed logic signals are modulated by the PLL's voltage controlled oscillator (VCO) output signal which operates at 384 times the ac line frequency. The two 30°-burst profile is formed by modulating the 120°-wide delayed logic signals with the VCO output and the output of a divide-by-64 counter.

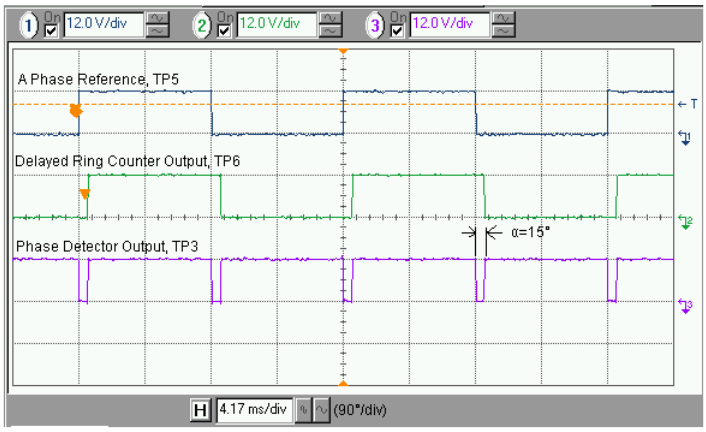

Figure 9. Phase Detector Signals, Phase A: α=15°
Channels: 1. Phase A Reference, TP5
2. Delayed Ring Counter Output, TP6
3. Phase Detector Output, TP3

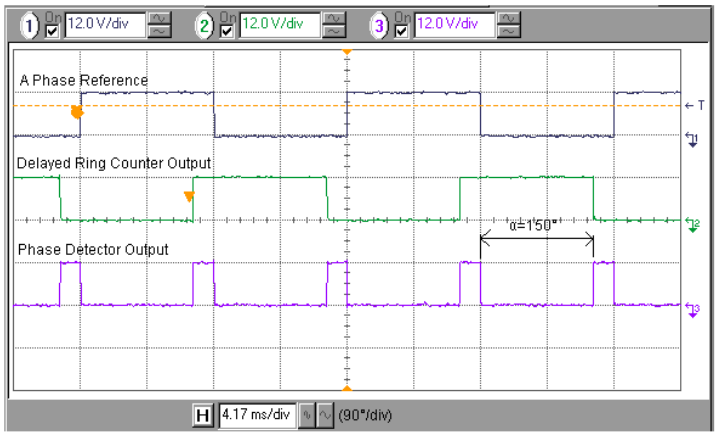

Figure 10. Phase Detector Signals, Phase A: α=150°
Channels: 1. Phase A Reference, TP5
2. Delayed Ring Counter Output, TP6
3. Phase Detector Output, TP3

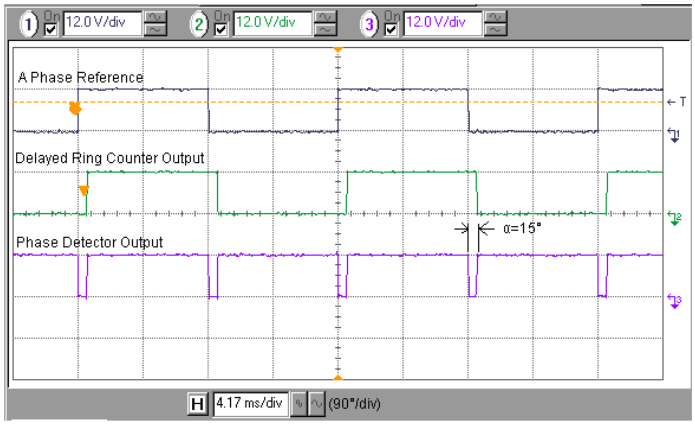

Figure 11. PLL Summing Amplifier Signals: α=15°
Channels: 1. Phase A Reference, TP5
2. Delayed Ring Counter Output, TP6
3. Phase Detector Output, TP3

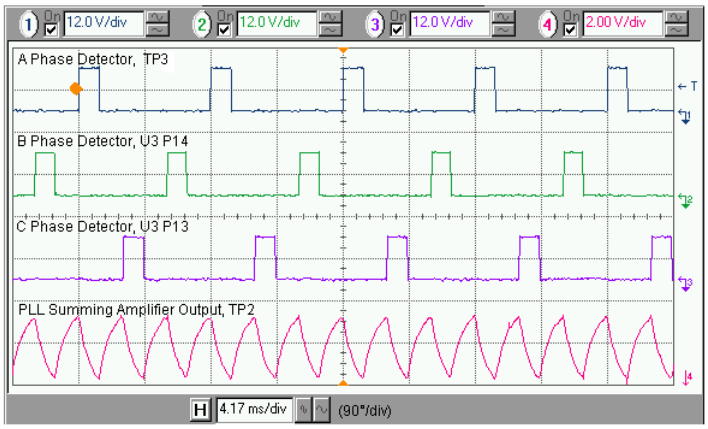

Figure 12. PLL Summing Amplifier Signals: α=150°
Channels: 1. A Phase Detector Output, TP3 (U3 P15)
2. B Phase Detector Output, U3 P14
3. C Phase Detector Output, U3 P13
4. Summing Amplifier Output, TP2

9.0 Gate Pulse Generation

The FCOG61BP gate pulse circuitry (see schematic E1535) consists of:

- Twelve IRFD110 MOSFETs, Q1 through Q12, which excite the primary of each pulse transformer. The gates of these MOSFETS are driven by the ASIC outputs.
- Resistors R3 through R8 and capacitors C2 through C7, which form the gate pulse shaping networks.
- Pulse modules PM1 through PM12, which provide current drive for the gate of each SCR. Each pulse module consists of a 2:1 ratio pulse transformer tested for 3500 V_{RMS} isolation, two secondary diodes, noise-suppression resistors across the primary and across the gate drive output, and a fusible link in series with the output. Each pulse module is potted in a silicone material.

10.0 Polarity Transition Circuit

10.1. Polarity Transition

The polarity transition command, or P signal, is located at J5 pin 5. This signal is normally pulled to 12 V through resistor RN9C, setting the firing polarity to the forward set of SCRs on J1 and J4. Pulling the P signal to 0 V sets the firing polarity to the reverse set of SCRs on J2 and J3. The POL TRANS polarity transition LED (PD3) blinks on each polarity transition, indicating that an effective polarity transition has taken place.

10.2. Polarity Transition Delay Time

In order to safely transition polarity, the polarity transition circuit must completely inhibit firing in either direction before firing the opposing set of SCRs. Additionally, the PT circuit must allow all SCRs to turn off or regenerate the energy in the load before firing commences in the opposite polarity.

The polarity transition delay time is the delay or dead time between a change of state in the P signal and the corresponding change in SCR gate firing polarity. The polarity transition delay is

adjustable by changing the time constant of R29 and C27. The minimum delay time required for a safe transition is 60ms; the maximum delay time can be extended to 20 seconds or greater as required by the specific application.

Certain applications may require load regeneration prior to polarity transition; this is usually a requirement when driving DC motors. In such cases, an external diode is installed between the SIG HI command and the $\overline{P \text{ XOR } P_D}$ signal (U9 pin 3).

10.3. Polarity Transition Inhibit Time and Soft-Stop Time

Immediately after assertion of the polarity transition command, the polarity transition circuit forces the board to inhibit by momentarily grounding $\overline{I_2}$ which soft-stops SCR firing. The soft-stop time constant, set by R28 and C17, must be selected such that firing is inhibited before the actual polarity transition takes place. This condition is typically configured and tested by Enerpro for any application-specific transition time.

10.4. Polarity Transition Soft-Start Time

Immediately after the actual transition, the polarity transition circuit releases $\overline{I_2}$, allowing the board to soft-start SCR firing. The soft-start time constant, set by the value of resistor R27 and capacitor C17, must be selected to give the desired soft-start time. The soft-start time is typically configured and tested by Enerpro for any customer specified transition time.

11.0 50/60 Hz Operation

The FCOG61BP revision C features a new compensation circuit that reduces delay angle variance with respect to frequency. The gate drive angle decreases approximately 5° for a frequency change from 60 to 50 Hz, whereas the delay angle of previous revisions decreased 12.5° over the same frequency range.

For operation with line frequencies in the range of 45 to 65 Hz, no modification to the frequency compensation circuit is required.

12.0 Electrical Specifications

Table 3. Specifications.

Maximum Ratings	
AC mains voltage	600 Vac
Pulse transformer hipot	3500 Vac (60 seconds)
Operating temperature range	-5 C to 85 C
Board ac supply voltage	28 Vac (24 Vac nominal)
12 V regulator output current	20 mA (Note 1)
5 V reference output current	5 mA (Note 1)
Auxiliary control power output from 24 Vac/30 VDC	10 W
Delay angle range	10° ≤ α ≤ 170°
Electrical Characteristics	
Delay angle command signal, SIG HI	Voltage: 0-5, 0.85-5.85, 0-10, 0-2 V Current: 4-20 mA Or per customer specification
Delay angle reference phase shift	0° or -30° (application-specific)
Control signal isolation from ground	653 kΩ (For higher isolation, use transformer coupled phase references)
Gate delay steady-state transfer function	Delay angle decreases as SIG HI increases
Gate delay dynamic transfer function bandwidth	-3 dB at 119 Hz, phase shift -45° at 68 Hz
Gate drive phase balance	±1° (max)
Delay angle variance	Δ(α)/Δ(f) = 0.5°/Hz
Mains voltage distortion effect	Firing not affected by zero crossing; phase reference filter attenuation is 12.8 dB relative to fundamental at 5^{th} harmonic
Lock acquisition time	30 ms (typ)
Soft-start/stop time (independently configurable)	0.05 – 20.0 s (typical)
Polarity transition inhibit time	0.06 – 20.0 s (typical)
Phase rotation effect	None
Phase loss inhibit	Automatic
Power-on inhibit	Automatic
Instant/soft inhibit/enable inputs	Dry contact
SCR gate pulse waveform (jumper selectable)	120° burst or 2-30° bursts, 30° spaced
Gate pulse burst frequency	384 times line frequency
Gate pulse width, 50 Hz	20-22 µs
Gate pulse width, 60 Hz	24-26 µs
Initial gate pulse open circuit voltage	15 V (Note 1)
Sustaining gate pulse open circuit voltage	7.0 V (Note 1)
Peak gate drive short circuit current	2.0 A (Notes 1 and 2)
Sustaining gate drive short circuit current	0.5 A (Notes 1 and 2)
Short-circuit gate drive current rise time	1.0 A/µs (Notes 1 and 2)
Board dimensions	194 x 191 x 34 mm (L x W x D)
Minimum creepage distance to ac mains	13 mm
Conformal coating	per MIL-1-46058, Type UR
Notes. 1. With nominal 30 Vdc supply. 2. With 1.0 Ω non-inductive gate load.	

13.0 Installation and Checkout

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCR unit. A 0-5V SIG HI delay angle command signal and onboard phase reference connections are assumed.

13.1. *Ensure that the ac mains are off.* Wire a plug, P2, with mains voltage connected to positions 2, 5, and 8. Insert plug P2 into connector J2.

13.2. Connect the appropriate input control power to J5: 24 Vac at J5 pin 1 and 2, or 30 V at J5 pin 3 and circuit common at J5 pin 11.

13.3. Install P5 with a 0-5 V SIG HI delay command signal, signal common, instant/soft inhibit controls, and polarity command wired to the plug.

13.4. Energize the firing board and apply the ac mains voltage.

13.5. Verify the presence of regulated 12 V ± 5% at J5 pin 6 and regulated 5 V ±5% at J5 pin 7 with a meter.

13.6. Verify that the PLL is in lock and the mains voltages are balanced by noting that the Phase Loss LED is not lit.

13.7. Verify that the average VCO control voltage at TP2 is approximately 5.0 V. This voltage is factory-set by selection of the VCO timing select resistor.

13.8. Determine the PLL gate delay angle from the pulse width of the A-phase detector output at TP3. If possible, calibrate the oscilloscope time-base at 20°/div (0.926 ms/div at 60 Hz) to read the gate delay angle directly off the horizontal axis.

13.9. Vary the delay command voltage from 0 VDC to 5.0 V. Verify that the gate delay angle at TP3 has the desired minimum and maximum values.

13.10. Reverse the polarity by grounding the polarity command at J5 pin 5. Verify that test point TP8 changes state inversely to the change in state of the polarity command. Observe that the POL TRANS polarity transition LED (PD3) blinks once when the polarity command changes state.