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Operating Manual: Six-SCR Variable Frequency General Purpose Gate Firing Board FCOVF6100 Revision J

Introduction

This manual describes the salient features and specifications of the FCOVF6100 firing board, including typical firing circuit signal waveforms and a checkout procedure.

Product Description

1.0 Application

The firing board responds to a voltage or current delay angle command signal (SIG HI) to produce a delayed set of six isolated, 60°-spaced high-current SCR gate firing pulses. Different configurations at different frequency ranges of operation are available for various types of SCR controllers or converters.

2.0 ASIC-Based Firing Circuit

All firing circuit logic is contained in a custom 24-pin ASIC. Additional detail on the firing circuit theory is contained in a separate engineering society paper[1].

3.0 Board Mounted Connectors

The firing board is connectorized to simplify maintenance and troubleshooting.

3.1. Gate/Cathode Connectors

Two 8-position Mate-N-Lok™ right-angle connectors[2], J1 and J2, provide the gate and cathode connections. The connectors are keyed to prevent incorrect installation or reversal of the mating plugs. Connector J1 accesses the gates and cathodes of the three SCRs having load-connected cathodes when the SCRs are arranged in the in-line ac controller or bridge converter configurations. Connector J2 accesses the gates and cathodes of the three SCRs having line-connected cathodes. Either P1 or P2 may be omitted as necessary if the firing board is used in a 3-SCR, 3-diode application.

3.2. Control Signal Connector

The firing board connects to the gate delay command and inhibit controls through a 15-position Mate-N-Lok™ connector J3. This connector also accesses the regulated (30 and 15 Vdc) output of the DC-DC Converter (if specified, otherwise regulated 30 and 15 Vdc must be supplied from an external regulated source), and the regulated +12/+5 Vdc outputs.

3.3. Power Supply Connector and Excitation

The FCOVF6100 accepts power from dual external 30 V/15 V supplies or from a single, external 24 or 48 V supply. Single-supply configurations utilize an onboard 20 W DC-DC converter rated for 1600 VDC isolation. With the DC-DC converter installed, board power is applied at positions 2 (positive) and 1 (negative) of J3 and approximately 10 watts are available from the 30 Vdc line (via J3 position 3) to power lamps, control relays, or other devices.

The DC-DC converter module is available with either 24 or 48 Vdc nominal input voltage. With the 24 V converter installed, the supply input voltage range is 18 to 36 Vdc. An onboard Zener diode pre-regulator circuit limits the converter's input voltage to a maximum of 30.6 Vdc. With the 48 Vdc converter installed, the supply input voltage range is 36 to 75 Vdc and the pre-regulator circuit limits the converter's input voltage to a maximum of 54.6 Vdc.

[1] Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.
[2] Vertical connectors are available upon request.

3.4. Optional Phase Reference Connector

In certain applications, the ac mains voltage may not be present at the SCR cathodes or the ac voltage may go to zero during load faults[3]. In these cases, or when galvanic isolation is required between power and control circuits, external phase reference voltages are applied through optional Mate-N-Lok™ connector J6 and voltage sensing resistors R5, R6 and R7. If the phase reference signals are obtained from the load-to-line SCRs at connector J2, resistors R5, R6, R7 and connector J6 must be omitted.

For onboard phase references from an external connection on J6, the pulse modules installed for PM1-PM6 are Enerpro part number EP1024-0. For onboard phase references from the SCR cathode connections, pulse modules PM4-PM6 are installed as in Table 1.

Table 1. Pulse Module Selection

Enerpro Part Number	Internal Phase Attenuation Resistor	Typical AC Mains Range
EP1024-0	None	N/A – Configured for external connection
EP1024-1	2.00 MΩ	300 – 600 Vac
EP1024-2	511 kΩ	150 – 300 Vac
EP1024-3	200 kΩ	30 – 150 Vac

3.5. Phase Reference Test Signal Input Connector

For low-power testing, users may connect low-level (5 V_{PP}) three-phase test reference signals to the three-position MTA header J5.

4.0 Gate Delay Command

The delay command signal, SIG HI, may be configured either as a 4 to 20 mA current command or one of several voltage commands. The default SIG HI range is 0 to 5 Volts. The input resistance presented to the delay command signal SIG HI is determined by resistors R24 & R25. The value of resistor R25 is selected as 10.0 kΩ when the control signal is designated as a control voltage. The buffer amplifier resistance table below lists the resistor values associated with different command signal levels. See also schematic diagram E0445 REV J.

Table 2. SIG HI Range vs. Buffer Amplifier Component Values

SIG HI Range	Resistance		
	R25	*R18*	*R24*
0 to 10 V	4.99 kΩ	45.3 kΩ	4.99 kΩ
0 to 5 V	10.0 kΩ	47.5 kΩ	0.0 Ω
4 to 20 mA	249 Ω	47.5 kΩ	0.0 Ω

5.0 Gate Inhibits

SCR gating is enabled by connecting either the instant inhibit, $\overline{I_1}$, to 12 V or by disconnecting the soft inhibit, $\overline{I_2}$, from ground. These signals are located at J3 pins 4 and 13, respectively. The instant inhibit signal $\overline{I_1}$ is pulled to ground through resistor R38 (1.50 kΩ). The user connects the $\overline{I_1}$ signal to 12 V to enable firing. This arrangement ensures that SCR gating is inhibited if plug P3 is inadvertently disconnected. A jumper may be installed between pins 4 and 6 of P3 to hold $\overline{I_1}$ at 12 V at all times in applications where the instant inhibit is not needed.

The soft inhibit signal $\overline{I_2}$ is pulled to 12 V through resistor R37 (1.50 kΩ). The user then grounds $\overline{I_2}$ to soft-stop SCR firing. In this mode, the delay angle is ramped from the setpoint value determined by SIG HI to the largest possible angle, after which firing is inhibited. This is termed the soft-stop shutdown mode. When user opens the connection at $\overline{I_2}$, gating is enabled with the delay angle set to the maximum limit. The delay angle then ramps to the value determined by SIG HI. The soft-stop and soft-start time constants are independently configurable via two timing

[3] For example, in a 6-SCR interphase transformer converter or an arc welder converter.

resistors (R33 and R34 respectively) and a capacitor (C25).

6.0 Phase Loss Inhibit

The FCOVF6100's phase loss circuit instantly inhibits SCR gating if the mains voltage phases are grossly imbalanced or if one or more phase voltages are missing. This feature also eliminates erratic response associated with voltage imbalance or transients when the three-phase mains are initially connected to the SCRs. The phase loss circuit is non-latching and soft-enables the board when the fault is cleared if the enable command is asserted. The phase loss circuit featured on the Revision J is immune to line frequency variations and transient voltages on the SIG HI line.

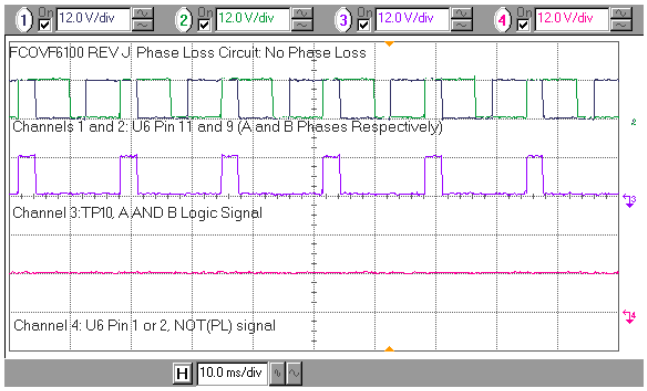

Figure 1. Phase Loss Circuit Signals – No Phase Loss[4]
Channels: 1. Digital A Phase Reference Signal, U6 P11
2. Digital B Phase Reference Signal, U6 P9
3. A and B logic signal, TP10
4. $\overline{PL}$ Signal, U6 P1

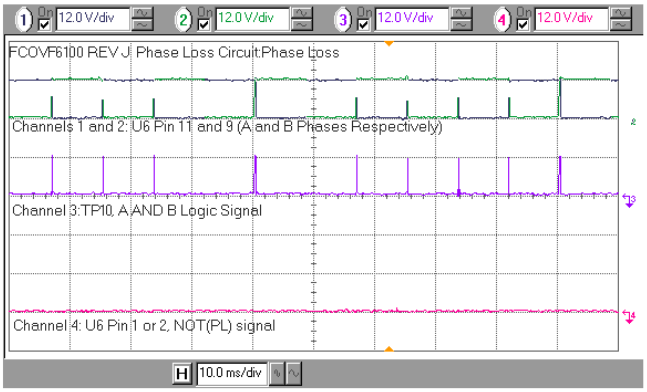

Figure 2. Phase Loss Circuit Signals – Phase Loss
Channels: 1. Digital A Phase Reference Signal, U6 P11
2. Digital B Phase Reference Signal, U6 P9
3. A and B logic signal, TP10
4. $\overline{PL}$ Signal, U6 P1

[4] All waveforms in this document were obtained with the FCOVF6100 firing board connected to 60 Hz, balanced 3-phase mains at pins 2, 5, and 8 of J2. The time base of some screenshots has been calibrated for phase measurements at 60 Hz. All component designations refer to drawing E445 Rev J.

7.0 Phase Reference Shift Selection

A first-order RC lowpass filter (formed by RN2 and capacitors C4, C5, and C6) shifts the mains phase references by 0° (for controller applications) or 60° lagging (for converter applications) at a nominal operating frequency of 60 Hz.

For 0° shifted references, C4-C6 are 0.033 uF film capacitors and RN2 is a 33 kΩ, three-position, isolated SIP resistor network. For 60° lagging references, RN2 is a 68 kΩ, three-position, isolated SIP resistor network (C4-C6 remain unchanged).

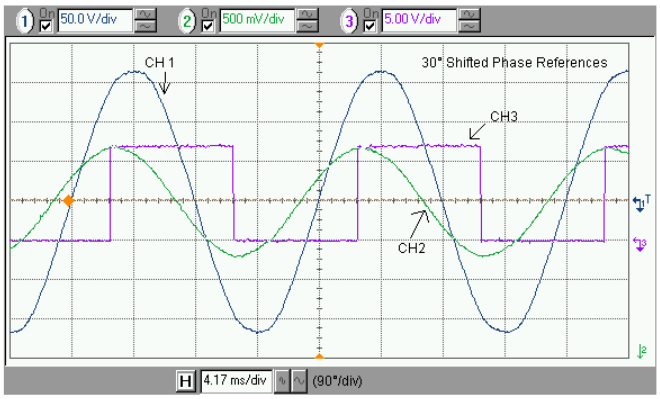

Figure 3. Sixty-degree shifted phase references, Phase A
Channel: 1. Phase A Line-to-Neutral Voltage
2. Attenuated and Filtered Mains Voltage at RN2 Pin 1
3. Reference Comparator Output, TP5

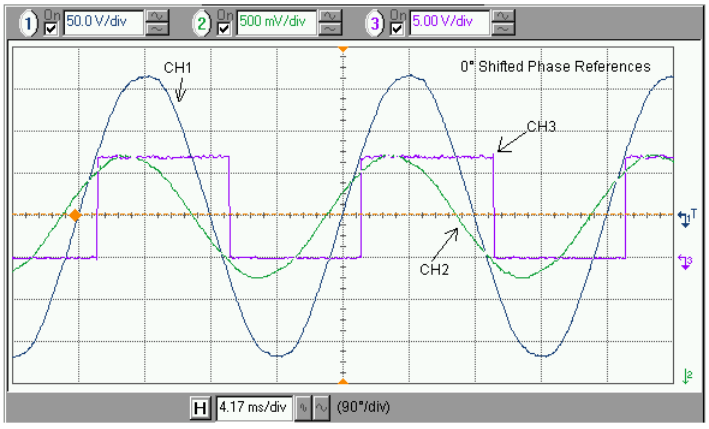

Figure 4. Zero-degree shifted phase references, Phase A
Channel: 1. Phase A Line-to-Neutral Voltage
2. Attenuated and Filtered Mains Voltage at RN2 Pin 1
3. Reference Comparator Output, TP5

8.0 Gate Pulse Generation

Two-position jumper JU1 enables gate pulse profile selection. With JU1 installed, the pulse profile is two 30°-wide bursts, each with an initial hard-firing gate pulse and followed by sustaining "picket fence" pulses. With the jumper omitted, the gate pulse profile changes to a single 120°-wide burst with the same hard-firing initial pulse. The initial hard-firing pulse and sustaining pulses ensure continuous SCR conduction over the required period.

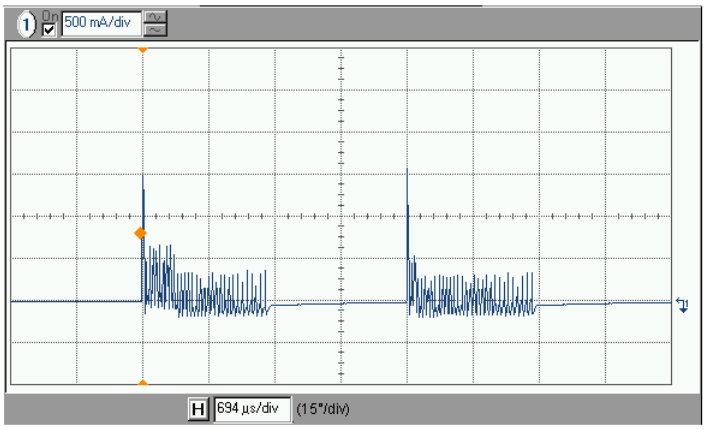

Figure 5. 2-30° Gate Pulse Profile (Into 1Ω)[5].

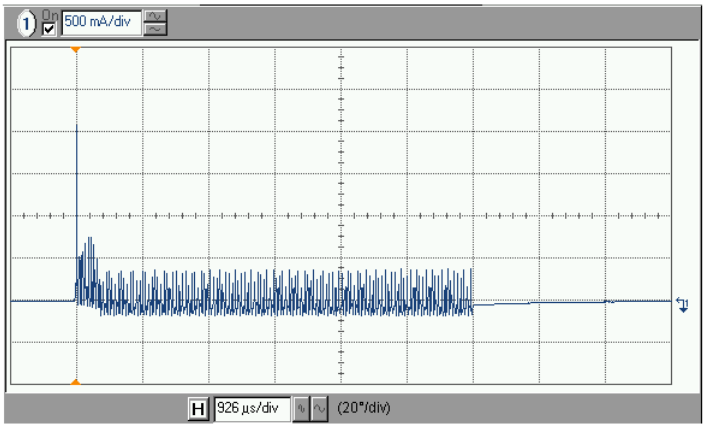

Figure 6. 120° Gate Pulse Profile (Into 1Ω).

[5] Current waveforms obtained using a Pearson model 2877 current transformer with 4 primary turns. The current transformer is terminated by the scope's 1.0 MΩ input impedance.

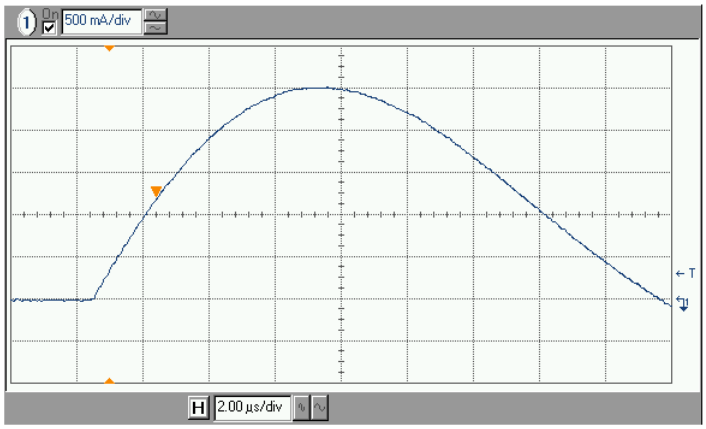

Figure 7. Initial pulse profile detail (Into 1Ω).

The firing circuit's phase-locked loop (PLL) locks the firing pulses to the three mains phases. A series of counters divide the PLL's oscillator output and a decoder section then generates six 120°- wide delayed logic signals. For the 120° single burst profile, the 120°-wide delayed logic signals are modulated by the PLL's voltage controlled oscillator (VCO) output signal which operates at 384 times the ac line frequency. The two 30°-burst profile is formed by modulating the 120°-wide delayed logic signals with the VCO output and the output of a divide-by-64 counter.

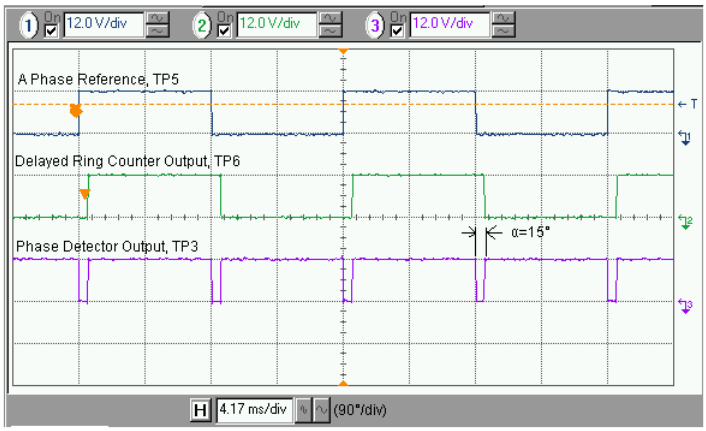

Figure 8. Phase Detector Signals, Phase A: α = 15°
Channels: 1. Phase A Reference, TP5
2. Delayed Ring Counter Output, TP6
3. Phase Detector Output, TP3

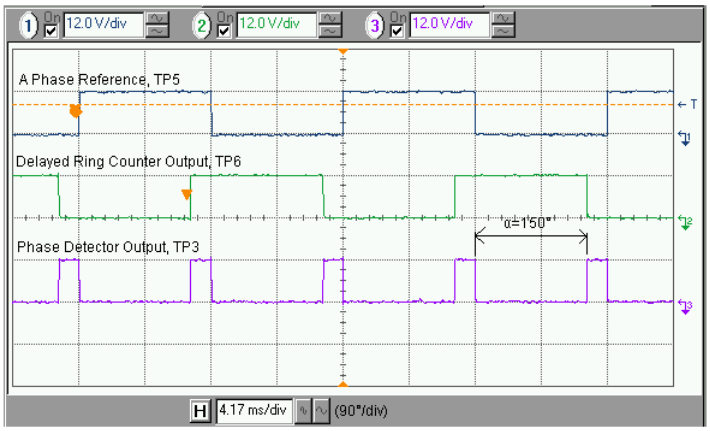

Figure 9. Phase Detector Signals, Phase A: α=150°
Channels: 1. Phase A Reference, TP5
2. Delayed Ring Counter Output, TP6
3. Phase Detector Output, TP3

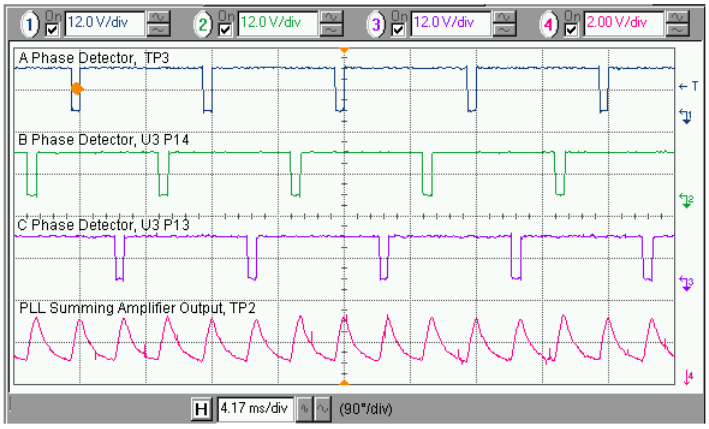

Figure 10. PLL Summing Amplifier Signals: α = 15°
Channels: 1. A Phase Detector Output, TP3 (U2 P15)
2. B Phase Detector Output, U2 P14
3. C Phase Detector Output, U2 P13
4. Summing Amplifier Output, TP2

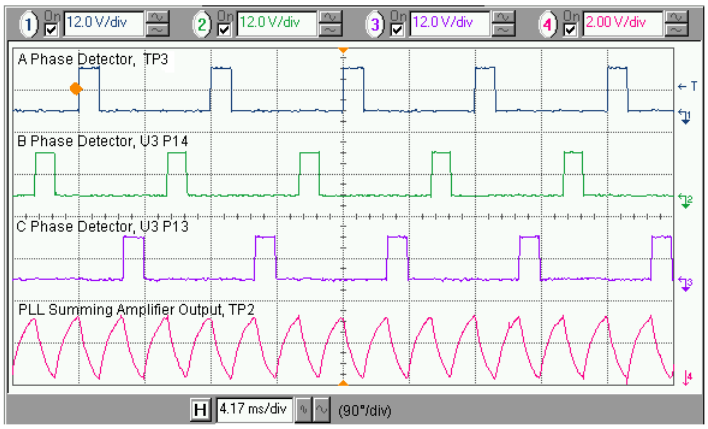

Figure 11. PLL Summing Amplifier Signals: α = 150°
Channels: 1. A Phase Detector Output, TP3 (U2 P15)
2. B Phase Detector Output, U2 P14
3. C Phase Detector Output, U2 P13
4. Summing Amplifier Output, TP2

The DDFOVF6100 (delay determinator fiber optic) is a version of the FCOVF6100 with fiber optic outputs replacing the pulse transformers. Six FO1024 modules are installed which feature Avago HFBR-1412Z fiber optic transmitters in lieu of the EP1024 modules. The transmitters feature ST (bayonet) style connectors, operate at 820 nm and are directly compatible with the MVTB series of medium voltage trigger boards. Each module has an LED to indicate that the fiber optic transmitter is operational. Please specify this configuration on your ordering documents or contact Enerpro for additional information.

9.0 Variable Frequency Range of Operation: Standard 30 – 140 Hz Range

The FCOVF6100 revision J features a new frequency compensation circuit that reduces delay angle variance with respect to frequency.

9.1 PLL and Gate Delay Angle Generation

Three 50% duty cycle phase reference signals are applied to EX-OR phase comparators in the LSI device along with three delayed phase references from the output of the PLL delay angle generator. A gate delay angle command voltage is summed with the outputs of the three phase detectors and low pass filtered by an inverting amplifier. This inverted voltage sum is applied to the control input of the LSI device as the Voltage Controlled Oscillator (VCO) control voltage.

At a given reference frequency, the sum of the control signal and the phase detector outputs is constant and the VCO is in lock with the mains voltage. To maintain phase lock, an increase in the control voltage must be accompanied by a decrease in the sum of the phase detector outputs. The delay between the three phase references and the three delayed output phase references of the PLL, which are input pairs to the three EX-OR phase detectors, thus tracks the control voltage.

9.2 Frequency Insensitivity

A frequency-to-voltage converter reduces the gate delay angle drive variance with respect to frequency. The VCO frequency is proportional to the current in the VCO timing resistor R13. For

the usual fixed-frequency operation, the sink for the current in R13 is the circuit common. The result is that the resistor current and the VCO frequency are proportional to the voltage across R13. The variable frequency modification consists of terminating R13 in a voltage source driven by the frequency-to-voltage converter instead of the usual circuit common.

The output of this voltage source is inversely proportional to the line frequency so that the voltage across the timing resistor increases with the line frequency. The sum of the phase detector outputs and the control voltage therefore remains unchanged. With a constant SIG HI voltage applied, the PLL delay angle variance is limited to less than 9° over the nominal 30 - 140 Hz frequency range.

9.3 Typical Delay Angles vs. Frequency

Typical delay angle ranges at different operating frequencies are listed in Table 3.

Table 3. Delay Angle Variance vs Line Frequency

Line Frequency	**TP3 Duty Cycle, %**	**Delay Angle, Deg**
SIG HI = 0 V, Δ α = 8.3°		
30	10.7	160.7
60	7.9	165.8
90	7.3	166.9
120	6.6	168.1
140	6.1	169.0
SIG HI = 2.5 V, Δ α = 6.6°		
30	51.8	86.8
60	48.8	92.2
90	48.6	92.5
120	47.4	94.7
140	48.1	93.4
SIG HI = 5.0 V, Δ α = 9.4°		
30	92.1	14.2
60	89.2	19.4
90	89.1	19.6
120	88.7	20.3
140	86.9	23.6

9.4 Custom Operating Frequency Ranges

For other frequency ranges of operation, please contact Enerpro engineering.

10.0 Electrical Specifications

Table 4. Specifications.

Maximum Ratings	
AC mains voltage	600 Vac
Pulse transformer hipot	3500 Vac (60 seconds)
Operating temperature range	-5 C to 85 C
Board supply voltages without DC-DC converter	30 and 15 VDC, ± 5%
Board supply input range with DC-DC converter, 24 VDC nominal input	18 - 36 VDC
Board supply input range with DC-DC converter, 48 VDC nominal input	36 - 75 VDC
12 V regulator output current	20 mA
5 V reference output current	5 mA
Auxiliary control power output from 30 VDC output	10 W
Delay angle range	10° ≤ α ≤ 170°
Electrical Characteristics	
Delay angle command signal, SIG HI	Voltage: 0-5, 0.85-5.85, 0-10, 0-2 V Current: 4-20 mA or per customer specification
Delay angle reference phase shift	-60° (or application-specific)
Control signal isolation from ground	653 kΩ
Gate delay steady-state transfer function	Delay angle decreases as SIG HI increases
Gate delay dynamic transfer function bandwidth	-3 dB at 119 Hz, phase shift -45° at 68 Hz
Gate drive phase balance	±1° (max)
Delay angle variance	Δ(α)/Δ(f) = 0.5°/Hz
Lock acquisition time	30 ms (typ)
Soft-start/stop time (independently configurable)	0.05 – 20.0 s (typical)
Phase rotation effect	None
Phase loss inhibit	Automatic
Power-on inhibit	Automatic
Instant/soft inhibit/enable inputs	Dry contact
SCR gate pulse waveform (jumper selectable)	120° burst or 2-30° bursts, 30° spaced
Gate pulse burst frequency	384 times line frequency
Initial gate pulse open circuit voltage	15 V
Sustaining gate pulse open circuit voltage	7.0 V
Peak gate drive short circuit current	2.0 A (1.0 Ω gate load)
Sustaining gate drive short circuit current	0.5 A (1.0 Ω gate load)
Short-circuit gate drive current rise time	1.0 A/µs (1.0 Ω gate load)
Board dimensions	191 x 152 x 35 mm (L x W x D)
Minimum creepage distance to ac mains **With onboard phase references** **With phase reference entry on J6**	 13 mm 10 mm
Conformal coating	per MIL-1-46058, Type UR

11.0 Installation and Checkout

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCR unit. A 48V DC-DC converter module for PS1 and 0 - 5 V SIG HI delay angle command signal is assumed.

11.1. *Ensure that the power is off.* Wire a plug, P2, with mains voltage connected to sockets 2, 5, and 8. Insert plug P2 into connector J2.

11.2. Connect the appropriate input power to J3 at pins 1 and 2 (–IN and +IN respectively) to energize the DC-DC converter. If omitted, supply regulated +30 Vdc and +15 Vdc at J3-3 and J3-8 respectively.

11.3. Install plug P3 with a 0-5 Vdc SIG HI delay command signal, signal common, and instant/soft inhibit controls wired to the plug.

11.4. If a DC-DC converter module is installed, verify the presence of regulated +30 VDC ± 5% at J3-3 and regulated +15 VDC ±5% at J3-8 with a multimeter.

11.5. Verify the presence of regulated +12 Vdc ± 5% at J3-6 and regulated +5 Vdc ±5% at J3-7 with a multimeter.

11.6. Energize the firing board and apply the AC mains voltage to the SCRs.

11.7. Verify that the PLL is in lock and the mains voltages are balanced by noting the Phase Loss LED is not lit.

11.8. Verify that the DC level of the VCO control voltage at TP2 is 5.0 VDC. This voltage is factory-set by selection of the VCO timing select resistor.

11.9. Determine the PLL gate delay angle from the pulse width of the A-phase detector output at TP3: Calibrate the oscilloscope time-base at 20°/div (0.926 ms/div at 60 Hz). Read the gate delay angle directly from the TP3 pulse off the horizontal axis. Alternatively, the delay angle may be calculated from the duty cycle D of TP3 as $\alpha = 180°(1-D)$.

11.10. Vary the delay command voltage from 0 VDC to 5.0 VDC. Observe that the gate delay angle at TP3 has the desired minimum and maximum values.